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PMIC5030 Power Management IC Standard

(From JEDEC Board Ballot JCB-25-69, formulated under the cognizance of the JC-40.1 subcommittee on Digital Logic Families and Applications, item 346.99C).

1 Scope

This standard defines the specifications of interface parameters, signaling protocols, and features for PMIC device as used for memory module applications. The designation PMIC5030 refers to the device specified by this document.

The purpose is to provide a standard for the PMIC5030 device for uniformity, multiplicity of sources, elimination of confusion, ease of device specifications, and ease of use.

Unless otherwise noted in this document, any illegal operation is not allowed and device operation is not guaranteed.

NOTE: The designation PMIC5030 refers to a portion of the part number designation of a series of commercial logic devices common in the industry. This number is normally preceded by a series of manufacturers specific characters to make up a complete part designation.

2 Description

The PMIC5030 is designed for typical DDR5 RDIMM and DDR5 MRDIMM as well as various types of CXL module application. The PMIC features six step down switching regulators and two LDO regulators (1.8V LDO and 1.0V LDO) for external usage and either one or two LDO regulators (VBIAS1 and VBIAS2) for PMIC's own internal consumption.

The PMIC is designed to support approximately 25 to 30 Watts of power. The PMIC is powered from VIN_Bulk input for switching regulators and VIN_Mgmt input for the rest of the PMIC. The PMIC supports selectable interface (I²C or I³C Basic) to fit various application environment. The PMIC device is intended to operate up to 12.5 MHz on a 1.0 V I³C Basic bus or up to 1 MHz on a 1.0 V to 3.3 V I²C bus.

2.1 Common Features Summary

Table 1 — PMIC Device Type Summary

| Device Type | SWA | SWB | SWC | SWD | SWE | SWF | Unit |
|------------------------------|-----|-----|-----|-----|-----|-----|------|
| Current Capability per Phase | 7.5 | 7.5 | 7.5 | 5 | 7.5 | 7.5 | A |

- VIN_Bulk input supply range: 4.25 V to 15.0 V
- VIN_Mgmt input supply range: 3.0 V to 3.6 V
- Six step down switching regulators: SWA, SWB, SWC, SWD, SWE, and SWF
- Programmable one three phase, two dual phase and six single phase regulator
- Three or Four LDO regulators: One or Two VBIAS (VBIAS1, VBIAS2), VOUT_1.8V, VOUT_1.0V

2.1 Common Features Summary (cont'd)

- Automatic switchover from VIN_Mgmt input supply to VIN_Bulk input supply
- Error injection capability
- Persistent Error log registers with detail information
- Write-protect mode and programmable of operation
- Independently programmable output voltages, power up and power down sequence for switch regulators
- Input and output power good status reporting mechanism
- VIN_Bulk input supply protection feature: Input over voltage
- Output switch regulators protection feature: Output over voltage, output under voltage, output current limiter
- Output current and power measurement, output current threshold mechanism
- Temperature measurement, temperature warning threshold, critical temperature shutdown
- Multi Time Programmable Non-Volatile Memory
- MTP Error Check capability
- Unique serial Number for traceability
- Programmable and DIMM specific registers for customization
- General Status Interrupt Function
- Reset input pin to reset various aspects of PMIC
- Auto Power On to turn on the regulators
- VR Output Enable Pin to turn on the regulators
- Flexible Open Drain IO (I²C) and Push Pull (I³C Basic) IO Support

3 Terms and Definitions

TBD

4 Package Pinout and Pin Description

4.1 Device Package Pinout

The PMIC5030 device is a 113 ball Flip Chip Fine Pitch BGA (FCBGA) with 11 x 13 ball grid, 0.5mm and 0.7mm ball pitch in x and y direction respectively. The package size is 5.55 mm x 9.0 mm nominal (5.6 mm x 9.05 mm maximum) as defined in MO-360, Terminal Pattern A. The ball diameter is 0.30 mm nominal; 0.25 mm minimum, 0.35 mm maximum.

4.2 Package Pinout

The PMIC pinout is shown in Table 2 for Bottom view. Pin A1 is bottom left in Table 2. Table 3 shows the PMIC pinout for Top view.

Ball pitch: 0.5 mm x 0.7 mm (x and y dimensions, respectively); Ball size (0.3 mm), SMD Pad SRO (0.275 mm); Package z-height 0.9 mm nominal (1.0 mm maximum).

Table 2 — Ball Assignment - 113 Ball FCBGA, 11 x 13 Grid, Bottom View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | |
|---|--------------|--------------|--------------|---------------|---------------|-------|--------------|-------------|--------------|--------------|--------------|---|
| N | PGND/ NC | PGND | PGND | VOUT_ 1.0V | VOUT_ 1.8V | AGND | VIN_ Mgmt | Reset_ n | PGND | PGND | PGND/ NC | N |
| M | SWA | SWA | PGND | PGND | SWA_F B | CAMP | SWC_ FB | PGND | PGND | SWC | SWC | M |
| L | SWA | SWA | SWA | PGND | | | | PGND | SWC | SWC | SWC | L |
| K | SWA_ BOOT | VIN_ Bulk | VIN_ Bulk | | | | | | VIN_ Bulk | VIN_ Bulk | SWC_ BOOT | K |
| J | SWB_ BOOT | VIN_ Bulk | VIN_ Bulk | | | GSI_n | | | VIN_ Bulk | VIN_ Bulk | SWF_ BOOT | J |
| H | SWB | SWB | SWB | PGND | SWB_ FB | AGND | SWF_ FB | PGND | SWF | SWF | SWF | H |
| G | SWB | SWB | PGND | PGND | | AGND | | PGND | PGND | SWF | SWF | G |
| F | PGND | PGND | PGND | | RFU2 | | RFU1 | | PGND | PGND | PGND | F |
| E | PGND | | | | SWE_ FB | AGND | SWD_ FB | | | | PGND | E |
| D | SWE_ BOOT | VIN_ Bulk | VIN_ Bulk | | | AGND | | | VIN_ Bulk | VIN_ Bulk | SWD_ BOOT | D |
| C | SWE | SWE | SWE | PGND | | | | PGND | SWD | SWD | SWD | C |
| B | SWE | SWE | PGND | PGND | RFU3 | SDA | SCL | PGND | PGND | SWD | SWD | B |
| A | PGND/ NC | PGND | PGND | VR_OE | VBIAS 1 | RFU4 | VBIAS 2 | PID | PGND | PGND | PGND/ NC | A |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | |

4.2 Package Pinout (cont'd)

Table 3 — Ball Assignment - 113 Ball FCBGA, 11 x 13 Grid, Top View

| | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |
|---|--------------|--------------|--------------|-------------|--------------|-------|---------------|--------------|--------------|--------------|--------------|---|
| N | PGND/ NC | PGND | PGND | Reset_ n | VIN_ Mgmt | AGND | VOUT_ 1.8V | VOUT_ 1.0 | PGND | PGND | PGND/ NC | N |
| M | SWC | SWC | PGND | PGND | SWC_ FB | CAMP | SWA_ FB | PGND | PGND | SWA | SWA | M |
| L | SWC | SWC | SWC | PGND | | | | PGND | SWA | SWA | SWA | L |
| K | SWC_ BOOT | VIN_ Bulk | VIN_ Bulk | | | | | | VIN_ Bulk | VIN_ Bulk | SWA_ BOOT | K |
| J | SWF_ BOOT | VIN_ Bulk | VIN_ Bulk | | | GSI_n | | | VIN_ Bulk | VIN_ Bulk | SWB_ BOOT | J |
| H | SWF | SWF | SWF | PGND | SWF_ FB | AGND | SWB_ FB | PGND | SWB | SWB | SWB | H |
| G | SWF | SWF | PGND | PGND | | AGND | | PGND | PGND | SWB | SWB | G |
| F | PGND | PGND | PGND | | RFU1 | | RFU2 | | PGND | PGND | PGND | F |
| E | PGND | | | | SWD_ FB | AGND | SWE_ FB | | | | PGND | E |
| D | SWD_ BOOT | VIN_ Bulk | VIN_ Bulk | | | AGND | | | VIN_ Bulk | VIN_ Bulk | SWE_ BOOT | D |
| C | SWD | SWD | SWD | PGND | | | | PGND | SWE | SWE | SWE | C |
| B | SWD | SWD | PGND | PGND | SCL | SDA | RFU3 | PGND | PGND | SWE | SWE | B |
| A | PGND/ NC | PGND | PGND | PID | VBIAS 2 | RFU4 | VBIAS 1 | VR_OE | PGND | PGND | PGND/ NC | A |
| | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |

4.2 Package Pinout (cont'd)

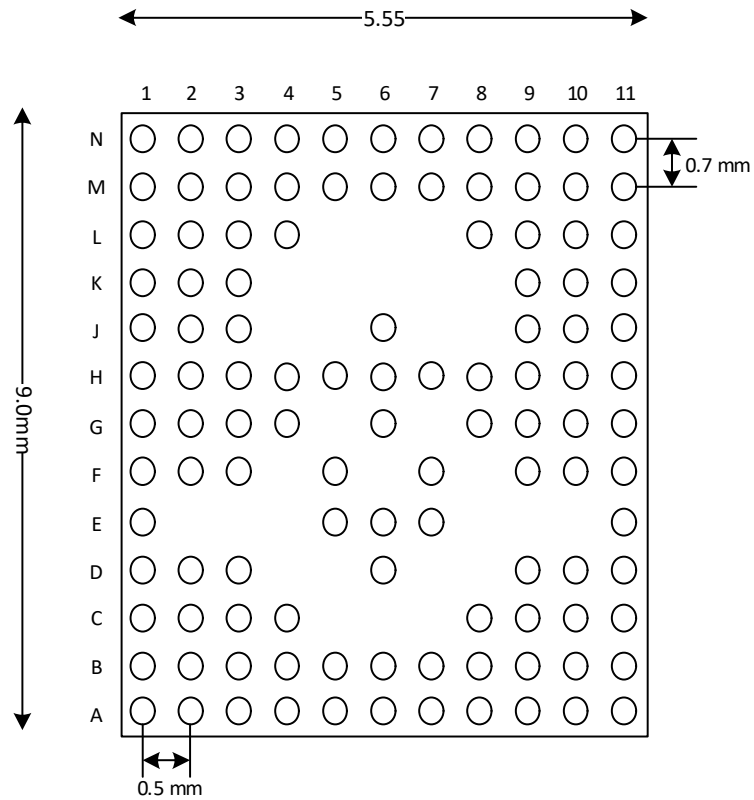


Figure 1 — Mechanical View - Bottom View

4.3 PMIC5030 Package Pin List

Table 4 — PMIC5030 Pin Description

| Pin Name | Type | Description |
|----------------|--------|--|
| VIN_Bulk (12x) | I, PWR | 12 V power input supply pin to the PMIC. All twelve VIN_Bulk input pins must be connected to the 12V input supply even if one or more output regulators are not intended to be used. |
| VIN_Mgmt | I, PWR | 3.3 V power input supply pin to the PMIC for VOUT_1.8V & VOUT_1.0V LDO outputs, sideband management access and internal PMIC operation. Vendor usage of 3.3V input supply may vary. |
| VBIAS1, VBIAS2 | O, PWR | <p>Vbias LDO output voltage generated by PMIC.</p> <p>PMIC vendors may choose to implement either one LDO output voltage regulator or two LDO output voltage regulators based on their design.</p> <p>If only one LDO output voltage regulator is used, the PMIC may internally tie VBIAS1 and VBIAS2 pin together or may use only VBIAS1 pin and ignore VBIAS2 pin.</p> <p>If two LDO output voltage regulators are used, the PMIC internally keeps VBIAS1 and VBIAS2 separate. However, there is only one common status register, threshold configuration register, clear and mask register for VBIAS. The ADC read out for both VBIAS1 and VBIAS2 LDO regulator is allowed.</p> <p>On DIMM PCB or any other application PCB, VBIAS1 and VBIAS2 pins are treated independently and each pin has its own de-coupling capacitors.</p> |
| CAMP | IO | <p>Control and Monitor Port.</p> <p>Open Drain Output: The PMIC floats this pin high when VIN_Bulk input supply, all enabled output buck regulators and all LDO regulator tolerance threshold is maintained as configured in the appropriate register. The PMIC drives this pin low when VIN_Bulk input goes below the threshold or when any of the enabled output buck regulator exceeds the threshold configured in the appropriate register or any LDO output regulator exceeds the threshold configured in the appropriate register.</p> <p>Input: The PMIC disables its output regulators when this pin transitions from high to low. The LDO outputs shall remain on.</p> <p>Input: The PMIC enters write-protect mode when the PMIC floats the CAMP output and it is pulled up High by external pullup resistor. The PMIC exits write-protect mode and enters in configuration mode when CAMP input is driven low to the PMIC externally.</p> |
| SCL | I | I ² C/I ³ C Basic Clock input for management bus. |
| SDA | IO | I ² C/I ³ C Basic Data Input/Output for management bus. |
| SWA | O | <p>Output switch node A buck regulator. This pin connects to L1 power inductor.</p> <p>In single phase regulator mode, the SWA output must not be connected to either SWB or SWC or SWE or SWF output even if they are configured as same exact output voltage.</p> <p>In dual phase regulator mode, the SWA+SWB output must not be connected to either SWC or SWE output or SWC+SWF output even if they are configured as same exact output voltage.</p> <p>In three phase regulator mode, the SWA+SWB+SWE output must not be connected to either SWC or SWE or SWC+SWF output even if they are configured as same exact output voltage.</p> |
| SWA_BOOT | PWR | Bootstrap node for SWA high side NMOS driver. This pin connects to SWA through a high quality capacitor. |
| SWA_FB | I | This pin connects to DIMM power plane load. |
| SWB | O | <p>Output switch node B buck regulator. This pin connects to L2 power inductor.</p> <p>In single phase regulator mode, the SWB output must not be connected to either SWA or SWC or SWE or SWF output even if they are configured as same exact output voltage.</p> <p>In dual phase regulator mode, the SWA+SWB output must not be connected to either SWC or SWE output or SWC+SWF output even if they are configured as same exact output voltage.</p> <p>In three phase regulator mode, the SWA+SWB+SWE output must not be connected to either SWC or SWF or SWC+SWF output even if they are configured as same exact output voltage.</p> |
| SWB_BOOT | PWR | Bootstrap node for SWB high side NMOS driver. This pin connects to SWB through a high quality capacitor. |
| SWB_FB | I | In single phase regulator mode, this pin connects to DIMM power plane load. In dual phase or three phase regulator mode, this pin must be connected to GND. |

Table 4 — PMIC5030 Pin Description (cont'd)

| Pin Name | Type | Description |
|------------|------|---|
| SWC | O | Output switch node C buck regulator. This pin connects to L3 power inductor. In single phase regulator mode, the SWC output must not be connected to either SWA or SWB or SWE or SWF or SWA+SWB output even if they are configured as same exact output voltage. In dual phase regulator mode, the SWC+SWF output must not be connected to either SWA or SWB or SWA+SWB or SWA+SWB+SWE output even if they are configured as same exact output voltage |
| SWC_BOOT | PWR | Bootstrap node for SWC high NMOS driver. This pin connects to SWC through a high quality capacitor. |
| SWC_FB | I | This pin connects to DIMM power plane load. |
| SWD | O | Output switch node D buck regulator. This pin connects to L4 power inductor. |
| SWD_BOOT | PWR | Bootstrap node for SWD high side NMOS driver. This pin connects to SWD through a high quality capacitor. |
| SWD_FB | I | This pin connects to DIMM power plane load. |
| SWE | O | Output switch node E buck regulator. This pin connects to L5 power inductor. In single phase regulator mode, the SWE output must not be connected to either SWA or SWB or SWC or SWF or SWA+SWB or SWC+SWF output even if they are configured as same exact output voltage. In three phase regulator mode, the SWA+SWB+SWE output must not be connected to either SWC or SWE or SWC+SWF output even if they are configured as same exact output voltage. |
| SWE_BOOT | PWR | Bootstrap node for SWE high side NMOS driver. This pin connects to SWE through a high quality capacitor. |
| SWE_FB | I | In single phase regulator mode, this pin connects to DIMM power plane load. In three phase regulator mode, this pin must be connected to GND. |
| SWF | O | Output switch node F buck regulator. This pin connects to L6 power inductor. In single phase regulator mode, the SWF output must not be connected to either SWA or SWB or SWE or SWC or SWA+SWB or SWA+SWB+SWE output even if they are configured as same exact output voltage. In dual phase regulator mode, the SWC+SWF output must not be connected to either SWA or SWB or SWA+SWB or SWA+SWB+SWE output even if they are configured as same exact output voltage |
| SWF_BOOT | PWR | Bootstrap node for SWB high side NMOS driver. This pin connects to SWF through a high quality capacitor. |
| SWF_FB | I | In single phase regulator mode, this pin connects to DIMM power plane load. In dual phase regulator mode, this pin must be connected to GND. |
| PID | I | PMIC ID pin for I ² C and I ³ C Basic bus. See Table 34 for ID definition. |
| VOUT_1.8V | O | 1.8V LDO Output. |
| VOUT_1.0V | O | 1.0 V LDO Output. |
| AGND (5x) | PWR | Analog Ground. Connects to DIMM ground plane. |
| PGND (38x) | PWR | Power Ground. Connects to DIMM ground plane. |
| VR_OE | I | PMIC Output Enable. If VR_OE pin function is disabled, this pin shall be pulled high through 200 K Ω resistor to VIN_Bulk on PCB. The PMIC does not turn on the regulators when this pin is high but does turn off the regulator if this pin is low. If VR_OE pin function is enabled, when this pin is high, the PMIC turns on the regulator and when this pin is low, the PMIC turns off the regulator. See clause 6.6 and 6.7 for details. This pin shall not be left floating. For typical DIMM application, this pin is always connected to VIN_Bulk through 200 K Ω on DIMM PCB. |
| Reset_n | I | Default Reset_n function - Active Low asynchronous reset input. CMOS input. When Low, it causes a reset to PMIC I ² C, I ³ C interface. |
| GSI_n | O | General Status Interrupt - Open Drain Output. The PMIC asserts this pin low to communicate any one or more events to host. This pin stays asserted until the appropriate registers are explicitly cleared. |
| RFU[1:4] | | These pins must be connected to GND. |

5 Electrical Specifications

5.1 Input Supply and Output Regulator Electrical Characteristics

5.1.1 Input Supply Electrical Characteristics

Table 5 — Input Supply DC + AC Specification

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|--|-----------------------|------|-----|-----|------|---------|
| Bulk Input Supply Voltage DC Voltage | VIN_Bulk | 4.25 | 12 | 15 | V | [1],[2] |
| Bulk Input Supply Maximum AC Voltage | VIN_Bulk_AC | - | - | 18 | V | |
| Bulk Input Supply Maximum Voltage Start up Overshoot | VIN_Bulk_OS_Startup | - | - | 33 | V*μs | [3] |
| Bulk Input Supply Voltage Ramp Up Rate | VIN_Bulk_Ramp_Up | 0.01 | - | 3.0 | V/ms | [4] |
| Bulk Input Supply Voltage Ramp Down Rate | VIN_Bulk_Ramp_Down | 0.01 | - | 1.0 | V/ms | [5] |
| Management Input Supply Voltage | VIN_Mgmt | 3.0 | 3.3 | 3.6 | V | [6] |
| Management Input Supply Ramp Up and Down Rate | VIN_Mgmt_Ramp | 0.15 | | 3 | V/ms | |
| Minimum Management Input Supply Current | I _{VIN_Mgmt} | 250 | - | - | mA | [7] |
| Bulk Input Supply Current | I _{VIN_Bulk} | | - | 4 | A | [8] |

- NOTE 1 During first power on, the input voltage supply must reach minimum value based on default from register [Table 131, Register 0x1A \[7:5\]](#) + 1.0V for PMIC to detect valid input supply.
- NOTE 2 The PMIC efficiency is optimized for nominal input supply of 12 V or lower. The PMIC efficiency above 13.8 V is degraded and thermal impact must be considered. The PMIC operation above 14.2 V should not be greater than 20% duty cycle at any time and should be limited to a maximum contiguous period of 10 minutes.
- NOTE 3 The area under the curve above VIN_Bulk = 15 V. VIN_Bulk_AC spec must also be satisfied.
- NOTE 4 The ramp up rate between 300 mV and 8.0 V.
- NOTE 5 The ramp down rate between 8.0 V and 300 mV.
- NOTE 6 During first power on, the input voltage supply must reach minimum value of 2.8 V for PMIC to detect valid input supply.
- NOTE 7 This is a platform spec. The minimum input current delivered by the platform through the DIMM gold finger to deliver the maximum load on LDO outputs (1.8V LDO output + 1.0V LDO output = 25 mA + 20 mA) plus the current required by the PMIC for its own usage.
- NOTE 8 This is a platform requirement spec. The maximum input supply voltage current requirement spec delivered by the platform through the DIMM gold finger.

5.1.2 Switch Regulator Output Electrical Characteristics

Table 6 — SWA, SWB, SWC, SWE, SWF - Single Phase Regulator; DC + AC Specification

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|--|----------------------|-------|-----|------|------|---------|
| Output Voltage | Vout | | 1.1 | | V | [1] |
| Maximum Continuous DC Current Load | I _{tdc} | 0 | - | 7.5 | A | [2] |
| Maximum Peak Instantaneous Current | I _{peakmax} | - | - | 9.5 | A | [3] |
| Maximum Load Transient | dI/dt | - | - | 7.5 | A/μs | [4] |
| Regulator Output DC + AC Voltage Tolerance | Reg_DC_AC_Tol | -2.5 | | 2.5 | % | [5],[6] |
| Regulator Feedback Set Point Accuracy | FB_Set_Point | -0.75 | | 0.75 | % | [7] |

NOTE 1 Typical voltage configured in appropriate register for SWA, SWB, SWC, SWE, and SWF.

NOTE 2 Measured over long period of time. Typically 1 second.

NOTE 3 Measured over short period of time. Typically $\geq 20 \mu\text{s}$ but less than $50 \mu\text{s}$.

NOTE 4 This parameter is applied to measure output voltage regulator DC+AC tolerance.

NOTE 5 The percentage applies to typical voltage configured in appropriate register. The PMIC bulk input supply voltage VIN_Bulk can vary from minimum to maximum value specified in [Table 5](#). The regulator output current load can vary maximum dI/dt value. The output ripple is inclusive in this parameter.

NOTE 6 Applies across entire PMIC operating temperature range.

NOTE 7 The percentage applies to typical voltage configured in the register and at a given temperature within operating temperature range. The PMIC bulk input supply voltage VIN_Bulk is fixed at nominal voltage of 12.0 V. The regulator output current load I_{tdc} = 0 A.

5.1.2 Switch Regulator Output Electrical Characteristics (cont'd)

Table 7 — SWA+SWB or SWC+SWF - Dual Phase^[1] Regulator; DC + AC Specification

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|--|----------------------|-------|-----|------|------|---------|
| Output Voltage | Vout | | 1.1 | | V | [2] |
| Maximum Continuous DC Current Load | I _{ldc} | 0 | - | 15 | A | [3] |
| Maximum Peak Instantaneous Current | I _{peakmax} | - | - | 19 | A | [4] |
| Maximum Load Transient | dI/dt | - | - | 15 | A/μs | [5] |
| Regulator Output DC + AC Voltage Tolerance | Reg_DC_AC_Tol | -2.5 | | 2.5 | % | [6],[7] |
| Regulator Feedback Set Point Accuracy | FB_Set_Point | -0.75 | | 0.75 | % | [8] |

- NOTE 1 Only applicable if Register [Table 247, Register 0x4F](#) [5,0] = '01' for SWA+SWB and [Table 247, Register 0x4F](#) [6] = '1' for SWC+SWF. The register setting in SWB and SWF is ignored by the PMIC.
- NOTE 2 Typical voltage configured in register [Table 138, Register 0x21](#) [7:1] for SWA+SWB and [Table 142, Register 0x25](#) [7:1] for SWC+SWF. The register setting in [Table 140, Register 0x23](#) [7:1] and [Table 187, Register 0x11F](#) is ignored by PMIC for dual phase operation.
- NOTE 3 Measured over long period of time. Typically 1 second.
- NOTE 4 Measured over short period of time. Typically $\geq 20 \mu\text{s}$ but less than $50 \mu\text{s}$.
- NOTE 5 This parameter is applied for the measurement of the output voltage regulator accuracy.
- NOTE 6 The percentage applies to typical voltage configured in the register. The PMIC bulk input supply voltage VIN_Bulk can vary from minimum to maximum value specified in [Table 5](#). The regulator output current load can vary maximum dI/dt value. The output ripple is inclusive in this parameter.
- NOTE 7 Applies across entire PMIC operating temperature range.
- NOTE 8 The percentage applies to typical voltage configured in the register and at a given temperature within operating temperature range. The PMIC bulk input supply voltage VIN_Bulk is fixed at nominal voltage of 12.0 V. The regulator output current load I_{ldc} = 0 A.

5.1.2 Switch Regulator Output Electrical Characteristics (cont'd)

Table 8 — SWA+SWB+SWE - Triple Phase^[1] Regulator; DC + AC Specification

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|--|----------------------|-------|-----|------|------|---------|
| Output Voltage | Vout | | 1.1 | | V | [2] |
| Maximum Continuous DC Current Load | I _{tdc} | 0 | - | 22.5 | A | [3] |
| Maximum Peak Instantaneous Current | I _{peakmax} | - | - | 28.5 | A | [4] |
| Maximum Load Transient | dI/dt | - | - | 22.5 | A/μs | [5] |
| Regulator Output DC + AC Voltage Tolerance | Reg_DC_AC_Tol | -2.5 | | 2.5 | % | [6],[7] |
| Regulator Feedback Set Point Accuracy | FB_Set_Point | -0.75 | | 0.75 | % | [8] |

NOTE 1 Only applicable if register [Table 247, Register 0x4F](#) [5] = '1' for SWA+SWB+SWE; the register [Table 247, Register 0x4F](#) [0] is a don't care.

NOTE 2 Typical voltage configured in register [Table 138, Register 0x21](#) [7:1] for SWA+SWB+SWE. The register setting in [Table 140, Register 0x23](#) [7:1] and [Table 185, Register 0x11D](#) [7:1] is ignored by PMIC for triple phase operation.

NOTE 3 Measured over long period of time. Typically 1 second.

NOTE 4 Measured over short period of time. Typically $\geq 20 \mu\text{s}$ but less than $50 \mu\text{s}$.

NOTE 5 This parameter is applied to measure output voltage regulator DC+AC tolerance.

NOTE 6 The percentage applies to typical voltage configured in the register. The PMIC bulk input supply voltage VIN_Bulk can vary from minimum to maximum value specified in [Table 5](#). The regulator output current load can vary maximum dI/dt value. The output ripple is inclusive in this parameter.

NOTE 7 Applies across entire PMIC operating temperature range.

NOTE 8 The percentage applies to typical voltage configured in the register and at a given temperature within operating temperature range. The PMIC bulk input supply voltage VIN_Bulk is fixed at nominal voltage of 12.0 V. The regulator output current load I_{tdc} = 0 A.

5.1.2 Switch Regulator Output Electrical Characteristics (cont'd)

Table 9 — SWD - Single Phase Regulator; DC + AC Specification

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|--|---------------|-------|-----|------|------|----------|
| Output Voltage | Vout | | 1.8 | | V | [1] |
| Maximum Continuous DC Current Load | Itdc | 0 | - | 5 | A | [2] |
| Maximum Peak Instantaneous Current | Ipeakmax | - | - | 6 | A | [3] |
| Maximum Load Transient | dI/dt | - | - | 5 | A/μs | [4] |
| Regulator Output DC + AC Voltage Tolerance | Reg_DC_AC_Tol | -2.5 | | 2.5 | % | [5], [6] |
| Regulator Feedback Set Point Accuracy | FB_Set_Point | -0.75 | | 0.75 | % | [7] |

NOTE 1 Typical voltage configured in register [Table 144, Register 0x27](#) [7:1].

NOTE 2 Measured over long period of time. Typically 1 second.

NOTE 3 Measured over short period of time. Typically $\geq 20 \mu\text{s}$ but less than $50 \mu\text{s}$.

NOTE 4 This parameter is applied to measure output voltage regulator DC+AC tolerance.

NOTE 5 The percentage applies to typical voltage configured in the register. The PMIC bulk input supply voltage VIN_Bulk can vary from minimum to maximum value specified in [Table 5](#). The regulator output current load can vary maximum dI/dt value. The output ripple is inclusive in this parameter.

NOTE 6 Applies across entire PMIC operating temperature range.

NOTE 7 The percentage applies to typical voltage configured in the register and at a given temperature within operating temperature range. The PMIC bulk input supply voltage VIN_Bulk is fixed at nominal voltage of 12.0V. The regulator output current load Itdc = 0 A.

5.1.3 Switch Regulator Efficiency

The PMIC5030 efficiency spec is defined for the reference test board only and it is not applicable for any application board which varies from the reference test board. The reference test board includes the inductor and the PCB characteristics which complies with the footnote 1 in Table 10. The efficiency spec is only measured for one switch regulator at a time; all other switch regulators must be disabled. The PMIC switching frequency must comply with the footnote 9 in Table 10. The typical application environment which deviates from the reference test board, all buck regulator are turned on simultaneously, carries external load on LDOs and signal interface pins may not be held static will have lower efficiency than defined in Table 10. The combination of all variations for application environment is not subject to the efficiency spec as defined in Table 10.

Table 10 — Efficiency Characteristics

| Switch Node Output | Efficiency (% of Max I_{tdc} Load) | | | Unit | Notes |
|--|--------------------------------------|-----------|-----------|------|--|
| | 25% | 50% | 100% | | |
| SWA or SWB or SWC or SWE or SWF (Single Phase Regulator Mode) | ≥ 87 | ≥ 91 | ≥ 89 | % | [1],[2],[3],[4],[5],[6] ,[7],[8],[9],[10] |
| SWA + SWB or SWC + SWF (Dual Phase Regulator Mode) | ≥ 87 | ≥ 91 | ≥ 89 | % | |
| SWA + SWB + SWE (Three Phase Regulator Mode_ | ≥ 87 | ≥ 91 | ≥ 89 | | |
| SWD | ≥ 87 | ≥ 92 | ≥ 89 | % | |

NOTE 1 VIN_Bulk = 12 V; VIN_Mgmt = 3.3 V

NOTE 2 The maximum I_{tdc} as specified in appropriate Tables above.

NOTE 3 When the efficiency of any given output regulator is being measured, all other switching output regulators are disabled.

NOTE 4 No external load on VOUT_1.8V, VOUT_1.0V LDO is applied.

NOTE 5 I²C/I³C Basic bus is pulled High and held static. CAMP and GSI_n signals are pulled High and held static.

NOTE 6 The efficiency includes the buck regulator loss, the PCB loss (≤ 2.5 m Ω) and see Section 9 for inductor specification for DCR and ACR.

NOTE 7 Efficiency calculation equation: $(V_{OUT} * I_{OUT}) / [(V_{IN_Bulk} * I_{IN_Bulk}) + (V_{IN_Mgmt} * I_{IN_Mgmt})]$; where V_{OUT} , I_{OUT} , V_{IN_Mgmt} , I_{IN_Mgmt} , V_{IN_Bulk} , I_{IN_Bulk} parameters are actual measured values.

NOTE 8 Applies at maximum ambient temperature of 65 °C (PMIC Junction temperature of 105 °C). The inductor characteristics noted above applies inductor temperature of 105 °C.

NOTE 9 The output buck regulator switching frequency must be set to 500 KHz. For all efficiency qualification testing, the device under test (DUT) must also comply with all PMIC's electrical characteristics (DC+AC) specifications.

NOTE 10 For input supply rails, probing is done at the input high frequency filter cap (0.1 μ F) to PMIC pin. For output rail, probing is done at the output cap location at the inductor load side.

5.1.4 LDO Output Regulator Characteristics

Table 11 — LDO Output Regulator DC + AC Specification

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|----------------------------|-----|-----|-----|------|-------|
| 1.8 V LDO Output Voltage | VOUT_1.8V | | 1.8 | | V | [1] |
| 1.8 V LDO Output - Maximum Output Current | I _{tdc_VOUT_1.8V} | - | - | 25 | mA | [2] |
| 1.0 V LDO Output Voltage | VOUT_1.0V | | 1.0 | | V | [3] |
| 1.0 V LDO Output - Maximum Output Current | I _{tdc_VOUT_1.0V} | - | - | 20 | mA | [4] |

NOTE 1 Typical voltage is configured in register [Table 148, Register 0x2B](#) [7:6]. The min and max values are guaranteed to be within ± 100 mV of programmed value.

NOTE 2 The maximum output current represents the external load and excludes PMIC's own internal current consumption. The specified maximum output current is only applicable after PMIC's 1.8V LDO Power Good status is good (i.e., t1.8V_Ready timing parameter is satisfied). Prior to PMIC's 1.8V LDO Power Good status (i.e., while PMIC is still ramping up the 1.8 V LDO, the maximum output current load shall be limited to maximum of 10 mA.

NOTE 3 Typical voltage is configured in register [Table 148, Register 0x2B](#) [2:1]. The min and max values are guaranteed to be within ± 50 mV of programmed value.

NOTE 4 The maximum output current represents the external load and excludes PMIC's own internal current consumption. The specified maximum output current is only applicable after PMIC's 1.0V LDO Power Good status is good (i.e., t1.0V_Ready timing parameter is satisfied). Prior to PMIC's 1.0V LDO Power Good status (i.e., while PMIC is still ramping up the 1.0V LDO), the maximum output current load shall be limited to maximum of 5 mA.

5.1.5 PMIC AC Timing Parameters

Table 12 — PMIC AC Timing Parameters

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|------------------------------------|-----------|-----|------|-------|-------|
| Input Supply to GSI_n assertion | tInput_PWR_GOOD_GSI_Assertion | | | 10 | μs | |
| Input over voltage condition to GSI_n assertion | tInput_OV_GSI_Assertion | - | - | 10 | μs | |
| Input over voltage condition to automatic PMIC VR Disable | tInput_OV_VR_Disable | - | - | 20 | μs | |
| Output Voltage Tolerance to GSI_n assertion | tOutput_PWR_GOOD_GSI_Assertion | - | - | 10 | μs | |
| Output over voltage condition to automatic PMIC VR Disable | tOutput_OV_VR_Disable | - | - | 20 | μs | |
| Output under voltage lockout condition to automatic PMIC VR Disable | tOutput_UV_VR_Disable | - | - | 20 | μs | |
| Output current limiter Warning to GSI_n assertion | tOutput_Current_Limiter | - | - | 10 | μs | |
| High Temperature Warning to GSI_n assertion | tHigh_Temp_Warning | - | - | 10 | μs | |
| Critical Temperature condition to automatic PMIC shut down | tShut_Down_Temp | - | - | 10 | μs | |
| VIN_Mgmt input supply stable to VR Enable Command | tVIN_Mgmt_to_Enable | 6.5 | - | - | ms | |
| VIN_Bulk input supply stable to VR Enable Command | tVIN_Bulk_to_Enable | 6.5 | - | - | ms | |
| VIN_Mgmt input supply stable to VOUT_1.8V output stable | t1.8V_Ready | - | - | 3.5 | ms | |
| VOUT_1.8V output supply stable to VOUT_1.0V output stable | t1.0V_Ready | - | - | 1.0 | ms | [1] |
| VOUT_1.8V output supply to PMIC Management Ready | tManagement_Ready | - | - | 3 | ms | |
| VR Enable Command to PMIC output regulator ready | tPMIC_PWR_Good_Out | Figure 16 | | | ms | |
| VR Disable Command to PMIC Output Regulators Off | tPMIC_Output_Off | Figure 20 | | | ms | |
| CAMP Input Low Pulse Width | tCAMP_Low_Pulse_Width | 2 | | | μs | |
| CAMP Input Low Pulse Width Input Filter | tCAMP_Low_Pulse_Width_Filter | - | - | 0.35 | μs | |
| VR_OE Input High/Low Pulse Width | tVR_OE_High_Low_Pulse_Width | 2 | | | μs | |
| VR_OE Input High/Low Pulse Width Filter | tVR_OE_High_Low_Pulse_Width_Filter | - | - | 0.35 | μs | |
| Output Voltage Adjustment in non-write-protect mode | $\Delta v/\Delta t$ | - | 1 | - | mV/μs | [2] |

NOTE 1 This time is added to t_1.8V_Ready parameter to get total time from VIN_Mgmt input supply.

NOTE 2 See footnote 4 for registers [Table 138, Register 0x21](#) [7:1], [Table 140, Register 0x23](#) [7:1], [Table 142, Register 0x25](#) [7:1], [Table 144, Register 0x27](#) [7:1]. The accuracy is $\pm 10\%$.

5.2 I²C, I³C Basic and Interface DC and AC Electrical Characteristics

Table 13 — I²C, I³C and Interface DC Electrical Specification

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|----------------------|------|-----|------|-------|
| Input Low Voltage (CAMP, SDA, SCL, VR_OE) | V _{IL} | -0.3 | 0.3 | V | |
| Input High Voltage (SDA, SCL) | V _{IH} | 0.7 | 3.6 | V | |
| Input High Voltage (CAMP) | V _{IH} | 1.26 | 3.6 | V | |
| Input High Voltage (VR_OE) | V _{IH} | 1.26 | 15 | V | |
| Output Low Voltage (SDA, GSI_n) | V _{OL} | - | 0.3 | V | [1] |
| Output High Voltage (SDA) | V _{OH} | 0.75 | - | V | |
| Output Low Current (SDA, GSI_n, CAMP) | I _{OL} | 3 | | mA | |
| Output High Current (SDA) | I _{OH} | - | -3 | mA | |
| Output Low Voltage (CAMP) | V _{OL_CAMP} | - | 0.3 | V | [2] |
| Rising Output Slew Rate (SDA) | Slew_Rate | 0.1 | 1 | V/ns | [3] |
| Falling Output Slew Rate (SDA) | | 0.1 | 3 | V/ns | |
| Input Leakage Current | I _{LI} | - | +5 | μA | |
| Output Leakage Current | I _{LO} | - | +5 | μA | |

NOTE 1 The pullup resistor for GSI_n signal may vary and is ≥ 1K Ohm.

NOTE 2 CAMP output is Open Drain output. There is an external pullup resistor to 3.3 V motherboard for standard DDR5 RDIMM/MRDIMM. For other DIMM environments, the external pullup resistor may be pulled to either 1.8V or 2.5V or 3.3V on either DIMM or the motherboard.

NOTE 3 Output slew rate is guaranteed by design and/or characterization. The output slew rate reference load is shown in Figure 7 and Figure 8 shows the timing measurement points. For slew rate measurement, the V_{OH} level shown in Figure 8 is a function of R_{on} value; V_{OH} = {1.0/(R_{on} + 50)} * 50.

Table 14 — CMOS Rail to Rail Input Levels for Reset_n

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|-----------------------|------|------|------|-------|
| AC Input High Voltage | V _{IH(AC)} | 0.88 | 1.1 | V | [1] |
| DC Input High Voltage | V _{IH(DC)} | 0.77 | 1.1 | V | [2] |
| AC Input Low Voltage | V _{IL(AC)} | VSS | 0.22 | V | [3] |
| DC Input Low Voltage | V _{IL(DC)} | VSS | 0.33 | V | [4] |
| Input Rise Time | t _{R_Reset} | - | 1.0 | μs | [5] |
| Peak to Peak voltage of slope reversal which must be suppressed | t _{SLPR_p2p} | - | 100 | mV | [5] |
| Peak to Peak width of slope reversal which must be suppressed | t _{SLPRPW} | - | 10 | ns | [5] |
| Input Reset Pulse Width | t _{PW_Reset} | 1.0 | | μs | [6] |

NOTE 1 The PMIC may experience overshoot. The overshoot is limited by the Absolute Maximum Ratings.

NOTE 2 Once Reset_n is registered High, Reset_n level must be maintained above V_{IH(DC)}, otherwise, the PMIC operation may not be guaranteed until it is reset asserting Reset_n signal Low.

NOTE 3 The PMIC may experience undershoot. The undershoot is limited by the Absolute Maximum Ratings

NOTE 4 After Reset_n is registered Low, Reset_n level shall be maintained below V_{IL(DC)} during t_{PW_Reset}, otherwise the PMIC may not be reset.

NOTE 5 The slope reversal (ringback) must remain below V_{SLPR_p2p} with the pulse width below t_{SLPRPW}.

NOTE 6 Clears registers as noted in clause 6.11.

5.2 I²C, I³C Basic and Interface DC and AC Electrical Characteristics (cont'd)

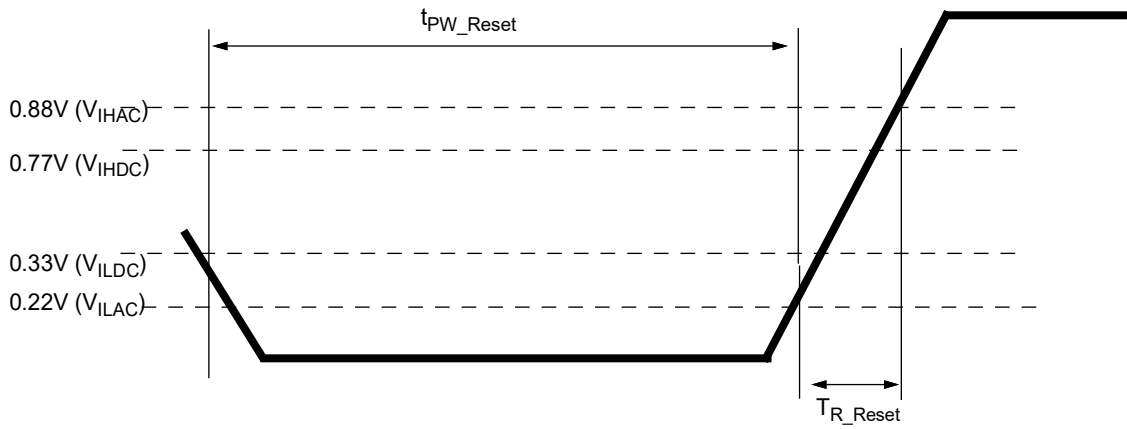
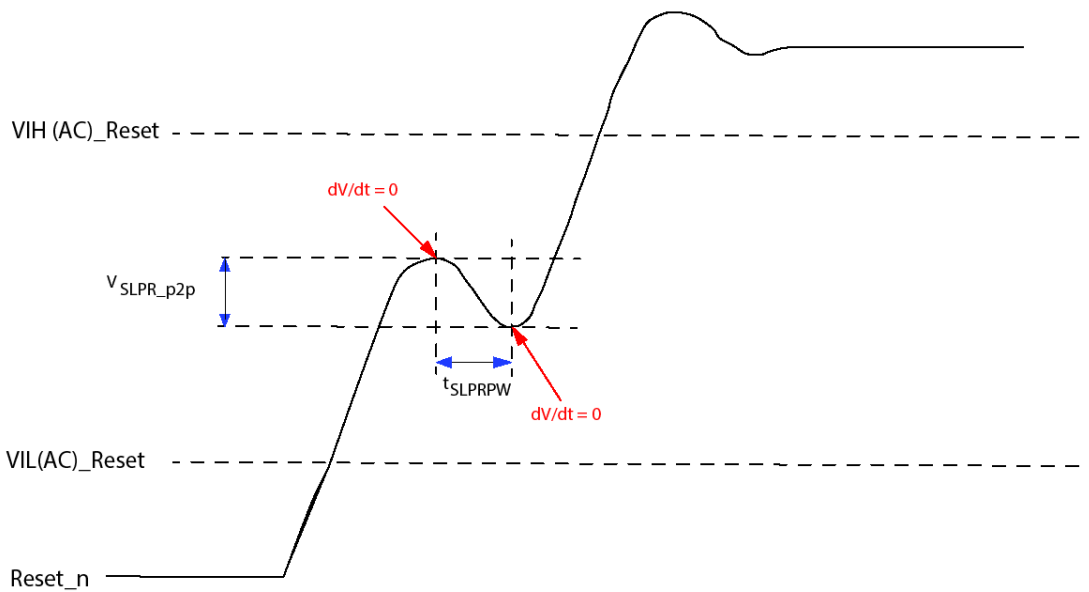


Figure 2 — Reset_n Input Slew Rate Definition



Note 1. Slope Reversal may occur anywhere between $V_{IL (AC)_Reset}$ and $V_{IH (AC)_Reset}$.
Note 2. There may be multiple ring backs within a single rising edge which the PMIC must be able to tolerate.

Figure 3 — Reset_n Slope Reversal Definition

Table 15 — Input Capacitance Spec

| Parameter | Symbol | Min | Max | Unit | Notes |
|--|----------|-----|-----|------|-------|
| Input Capacitance (CAMP, SCL, SDA, VR_OE, Reset_n) | C_{IN} | - | 5 | pF | |

5.2 I²C, I³C Basic and Interface DC and AC Electrical Characteristics (cont'd)

Table 16 — Input Spike Filter Spec

| Parameter | Symbol | Test Condition | Min | Max | Unit | Notes |
|---|-----------------|----------------------------|-----|-----|------|-------|
| Pulse width of spikes which must be suppressed by the input filter in I ² C mode | t _{SP} | Single glitch, f ≤ 100 KHz | - | - | ns | |
| | | Single glitch, f > 100 KHz | 0 | 50 | ns | [1] |

NOTE 1 T_A = 25 °C; f = 400 KHz. Verified by design and characterization only.

Table 17 — Output Ron

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|-----------------|-----|-----|------|-------|
| SDA Output Pullup and Pulldown Driver Impedance | R _{ON} | 20 | 100 | Ω | [1] |
| GSI_n, CAMP Output Pulldown Driver Impedance | | 20 | 100 | Ω | 1 |

NOTE 1 Pulldown Ron = V_{out}/I_{out}. Pullup Ron = (V_{OUT_1.0V} - V_{out})/I_{out}.

Table 18 — I²C and I³C Interface AC Characteristics

| Parameter | Symbol | I ² C Mode - Open Drain | | I ³ C Basic Mode Push-Pull ^[1] | | Unit | Notes |
|---|-------------------------|------------------------------------|-----|--|------|------|----------|
| | | Min | Max | Min | Max | | |
| Clock Frequency | f _{SCL} | 0.01 | 1 | 0.01 | 12.5 | MHz | |
| Clock High Pulse Width Time | t _{High} | 260 | | 35 | | ns | |
| Clock Low Pulse Width Time | t _{Low} | 500 | | 35 | | ns | |
| Detect Clock Input Low Time | t _{TIMEOUT} | 10 | 50 | 10 | 50 | ms | |
| Rise Time | t _R | - | 120 | - | 5 | ns | [2],[3] |
| Fall time | t _F | - | 120 | 0 | 5 | ns | 2,3 |
| Data in Setup Time | t _{SU:DAT} | 50 | - | 8 | - | ns | 2,[4] |
| Data in Hold Time | t _{HD:DI} | 0 | - | 3 | - | ns | 2,4 |
| Start Condition Setup Time | t _{SU:STA} | 260 | - | 12 | - | ns | 2 |
| Start Condition Hold Time | t _{HD:STA} | 260 | - | 30 | - | ns | 2 |
| Stop Condition Setup Time | t _{SU:STO} | 260 | - | 12 | - | ns | 2 |
| Time between Stop Condition and next Start Condition | t _{BUF} | 500 | - | 500 | - | ns | 2,[5] |
| SDA Data Out Hold Time | t _{HD:DAT} | 0.5 | 350 | N/A | N/A | ns | [6] |
| SCL Falling Clock In to Valid SDA Data Out Time | t _{DOUT} | N/A | N/A | 0.5 | 12 | ns | [7],[8] |
| SCL Rising Clock In to Target SDA Output Off | t _{DOFFT} | N/A | N/A | 0.5 | 12 | ns | 7,8,[9] |
| SCL Rising Clock In to Controller SDA Output Off | t _{DOFFC} | N/A | N/A | 0.5 | 30 | ns | 7,8,[10] |
| SCL Rising Clock In to Controller Driving Data Signal Low | t _{CL_r_DAT_f} | N/A | N/A | 40 | - | ns | [11] |

Table 18 — I²C and I³C Interface AC Characteristics (cont'd)

| Parameter | Symbol | I ² C Mode - Open Drain | | I ³ C Basic Mode Push-Pull ^[1] | | Unit | Notes |
|--|---------------------------------------|------------------------------------|-----|--|-----|------|----------------|
| | | Min | Max | Min | Max | | |
| Bus Available Time (no edges seen on SCL and SDA) | t _{AVAIL} | N/A | N/A | 1 | - | μs | |
| Time to issue IBI after an event is detected when Bus is available | t _{IBI_ISSUE} | N/A | N/A | - | 15 | μs | |
| Time from Clear Register Status to any I ³ C Basic operation with Start condition to avoid false IBI generation; PEC disabled | t _{CLR_I3C_CMD_Delay} | N/A | N/A | 4 | - | μs | |
| Time from Clear Register Status to any I ³ C Basic operation with Start condition to avoid false IBI generation; PEC enabled | | N/A | N/A | 15 | - | μs | |
| DEVCTRL CCC Followed by DEVCTRL CCC or Register Read/Write Command Delay | t _{DEVCTRLCCC_DELAY_PEC_DIS} | 3 | - | 3 | - | μs | [12],[13],[14] |
| Register Write Command Followed by Register Read Command Delay in PEC Enabled Mode | t _{WR_RD_DELAY_PEC_EN} | N/A | N/A | 8 | - | μs | [15],[16],[17] |
| SETHID CCC or SETAASA CCC followed by any other CCC or Read/Write Command Delay | t _{I2C_CCC_Update_Delay} | 2.5 | - | - | - | μs | |
| RSTDAA CCC or ENEC CCC or DISEC CCC to any other CCC or Read/Write Command Delay | t _{I3C_CCC_Update_Delay} | - | - | 2.5 | - | μs | |
| Any CCC followed by RSTDAA CCC delay | t _{CCC_Delay} | N/A | N/A | 2.5 | - | μs | |

NOTE 1 I³C mode with Open Drain operation follows timing values as shown in I²C Mode - Open Drain column.

NOTE 2 See Figure 4 for PMIC's input timing definition.

NOTE 3 See Figure 9 for voltage threshold definition for rise and fall times.

NOTE 4 The input setup time is referenced from SDA VIL or VIH threshold as shown in Figure to SCL VIH threshold as shown in Figure 4. The input hold time is referenced from SCL VIL threshold as shown in Figure 4 to SDA VIL or VIH threshold as shown in Figure 4.

NOTE 5 If PEC is enabled, t_{WR_RD_DELAY_PEC_EN} timing parameter applies.

NOTE 6 The PMIC device guarantees t_{HD:DAT} value in I²C mode of operation. See Figure 6 for PMIC's output timing definitions as well as SCL clock input threshold level and SDA data output threshold levels.

NOTE 7 The PMIC device must be configured in I³C Basic mode to guarantee t_{DOUT} or t_{DOFFT} or t_{DOFFC} value. See Figure 5 for PMIC's output timing definition as well as SCL clock input threshold level and SDA data output threshold levels.

NOTE 8 This timing parameter is guaranteed into output timing reference load as shown in Figure 7.

NOTE 9 The PMIC device must be configured in I³C Basic mode to guarantee t_{DOFFT} value. See Figure 22.

NOTE 10 The PMIC device must be configured in I³C Basic mode to guarantee t_{DOFFC} value. See Figure 23.

NOTE 11 See Figure 24.

NOTE 12 From STOP condition of DEVCTRL CCC to START condition for Register Read or Register Write Command Data Packet delay.

NOTE 13 The PMIC sends NACK if Host does not satisfy t_{DEVCTRLCCC_DELAY_PEC_DIS} timing parameter.

NOTE 14 This timing parameter restriction is only applicable when PEC function is disabled in PMIC. If PEC is enabled, this timing parameter does not apply.

NOTE 15 From STOP condition for Register Write Command Data Packet to START condition for Register Read Command Data Packet delay.

NOTE 16 This timing parameter restriction is only applicable when PEC function is enabled in PMIC. If PEC is disabled, this timing parameter does not apply.

NOTE 17 The PMIC sends NACK if Host does not satisfy t_{WR_RD_DELAY_PEC_EN} timing parameter.

5.2 I²C, I³C Basic and Interface DC and AC Electrical Characteristics (cont'd)

The PMIC device follows the I²C or I³C Basic bus timing requirements. The [Figure 4](#), [Figure 5](#), and [Figure 6](#) show the timing diagram for Data bus Input and Data Output parameters.

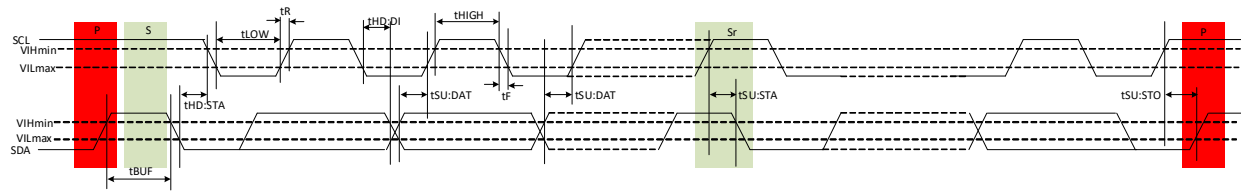


Figure 4 — I²C or I³C Basic Bus AC Input Timing Parameter Definition

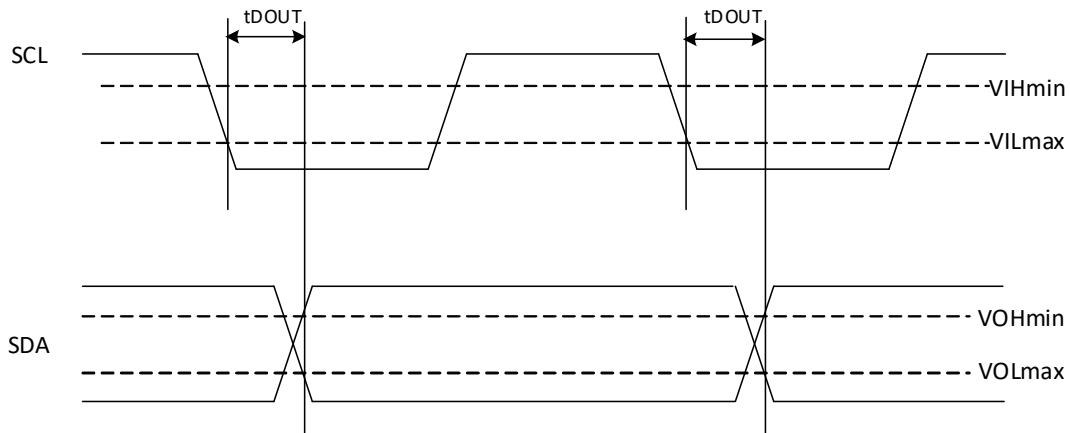


Figure 5 — I³C Basic Bus AC Data Output Timing Parameter Definition

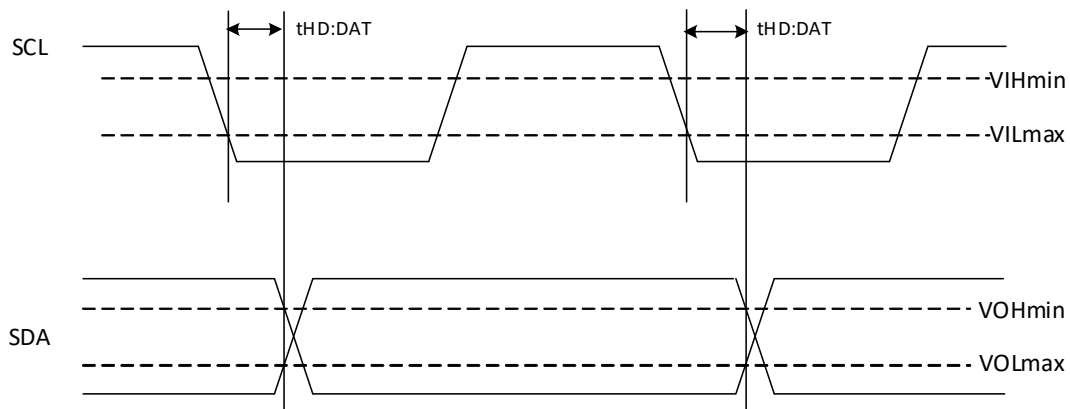


Figure 6 — I²C Bus AC Data Output Timing Parameter Definition

5.2 I²C, I³C Basic and Interface DC and AC Electrical Characteristics (cont'd)

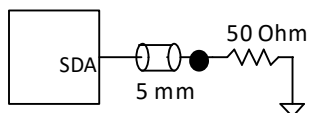


Figure 7 — Output Slew Rate and Output Timing Reference Load

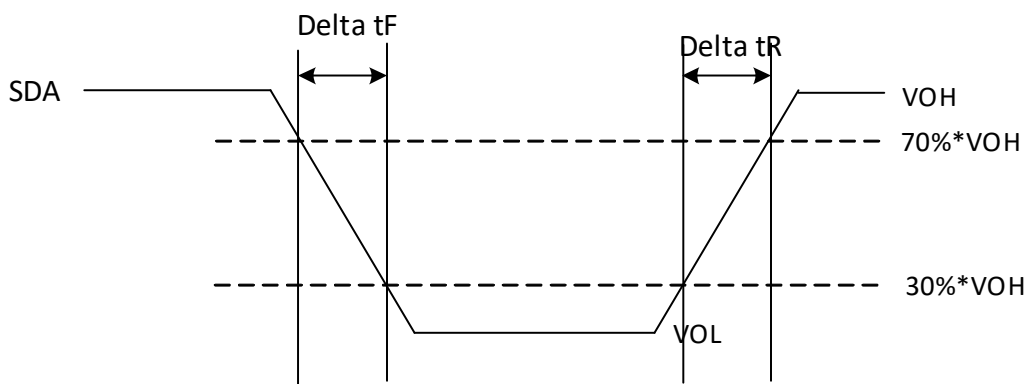


Figure 8 — Output Slew Rate Measurement Points

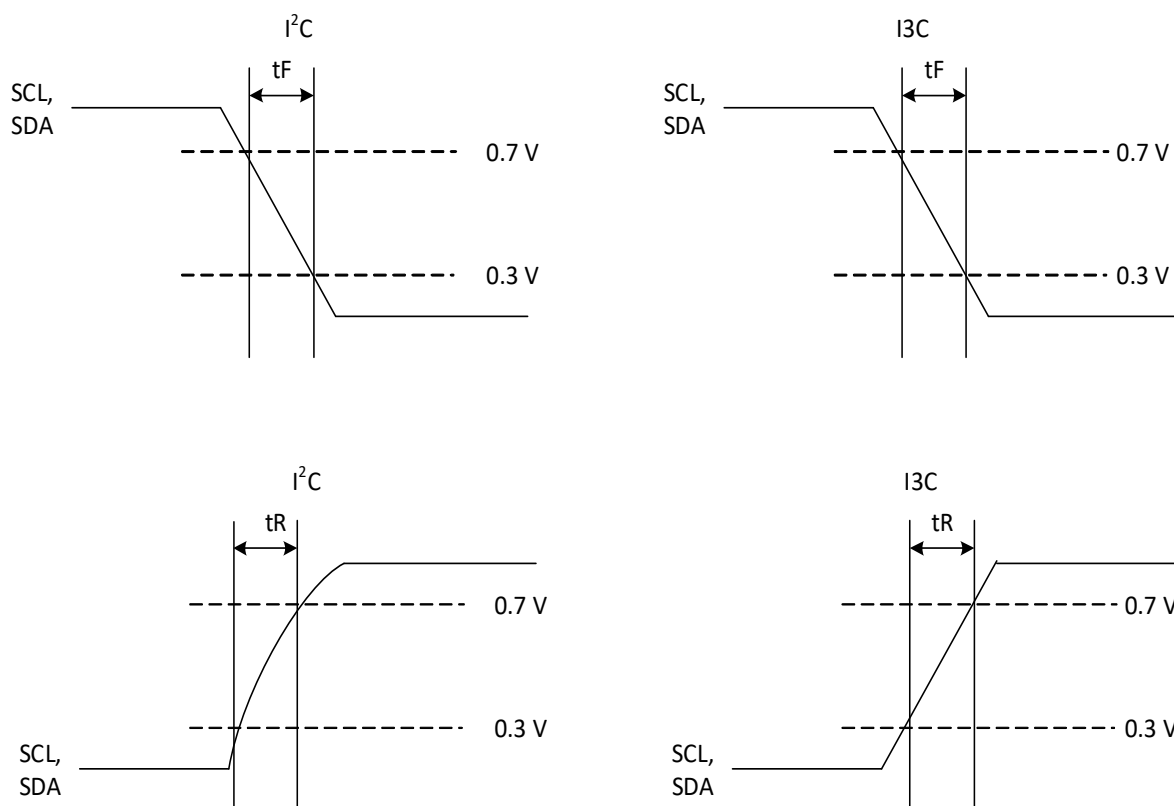


Figure 9 — Rise and Fall Timing Parameter Definition

5.2 I²C, I³C Basic and Interface DC and AC Electrical Characteristics (cont'd)

Table 19 — AC Measurement Conditions^[1]

| Symbol | Parameter | Min | Max | Units |
|----------------|--|------------|-----|-------|
| C _L | Load capacitance | | 40 | pF |
| | Input rise and Fall times - Open Drain | - | TBD | ns |
| | Input rise and fall times - Push Pull | - | TBD | ns |
| | Input signal swing levels | 0.2 to 0.8 | | V |
| | Input and Output timing reference levels | 0.3 to 0.7 | | V |

NOTE 1 These AC measurement conditions (Table 19 and Figure 10) are only for lab test purposes.

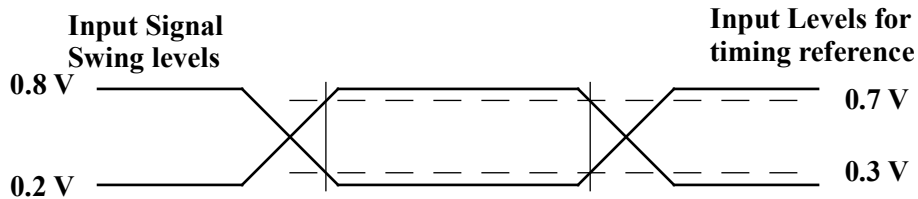


Figure 10 — AC Measurement Waveform

5.3 Thermal Characteristics

Table 20 — Thermal Characteristics

| Parameter | Symbol | Maximum Rating | Unit | Notes |
|-------------------------------------|-------------------|----------------|-----------------------------|-------------|
| Thermal resistance junction to case | Θ_{JC} | TBD | $^{\circ}\text{C}/\text{W}$ | [1],[2],[3] |
| Junction operating temperature | T _J | -10 to 125 | $^{\circ}\text{C}$ | |
| Case operating temperature | T _C | -10 to TBD | $^{\circ}\text{C}$ | 4 |
| Storage temperature | T _{STG3} | -55 to 150 | $^{\circ}\text{C}$ | 4 |
| Lead temperature (soldering, 10s) | T _{LEAD} | 300 | $^{\circ}\text{C}$ | [4] |

NOTE 1 The maximum power dissipation is $P_{D(\text{MAX})} = (T_{J\text{MAX}} - T_C) / \Theta_{JC}$. Exceeding the maximum allowable power dissipation results in excessive die temperature and the device will enter thermal shutdown.

NOTE 2 This thermal rating was calculated on JEDEC 51 standard 4 layer board with dimensions 3" x 4.5" in still air conditions. Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude and other unlisted variables.

NOTE 3 This specification is compliant with JESD402-1 Temperature Grade and Measurement Specification for Components and Modules, operating temperature range MT, storage temperature T_{STG3}. See JESD402-1 for details, including measurement point.

NOTE 4 Soldering temperature, 10 s.

5.4 Absolute Maximum Rating

The absolute maximum ratings are stress ratings only. Stresses greater than those listed in [Table 21, Absolute Maximum Rating](#), [Table 22, ESD Requirement](#), and [Table 23, EOS Requirement](#) may cause permanent damage to the device. Functional operation of the PMIC at absolute maximum ratings is not implied. Exposure to absolute maximum rating condition for extended periods may affect long term reliability.

Table 21 — Absolute Maximum Rating

| Pin | Maximum Rating | | Unit |
|---|----------------|-------------------------------|------|
| | DC | AC | |
| VIN_BULK, VR_OE | -0.3 to 16.2 | TBD (Duration \leq 25 ns) | V |
| VIN_Mgmt, VBIAS1, VBIAS2 | -0.3 to 6.0 | - | V |
| VOUT_1.8V, VOUT_1.0V | -0.3 to 2.2 | - | V |
| SWA, SWB, SWC, SWD, SWE, SWF | -0.3 to 16.2 | -4.5 to 20 (Duration < 25 ns) | V |
| SWA_BOOT, SWB_BOOT, SWC_BOOT, SWD_BOOT, SWE_BOOT, SWF_BOOT (to GND) | -0.3 to 21.0 | -0.3 to 24 (Duration < 25 ns) | V |
| SWA_BOOT, SWB_BOOT, SWC_BOOT, SWD_BOOT, SWE_BOOT, SWF_BOOT (to SWx) | -0.3 to 6.0 | TBD | V |
| SWA_FB, SWB_FB, SWC_FB, SWD_FB, SWE_FB, SWF_FB (to AGND) | -0.3 to 2.2 | - | V |
| PID | -0.3 to 2.2 | - | V |
| CAMP ^[1] , GSI_n, Reset_n | -0.3 to 5.0 | - | V |
| SCL, SDA; I ² C Mode only | -0.3 to 5.0 | TBD | V |
| SCL, SDA; I ³ C Mode only | -0.3 to 2.1 | TBD | V |
| AGND, PGND | -0.3 to 0.3 | - | V |

NOTE 1 CAMP pins shall withstand the stress when connected to maximum of 15 V DC source through 250 Ohm series resistor for 10 seconds.

Table 22 — ESD Requirement

| Test Model | Pin | Maximum Rating | Unit |
|------------|-----|----------------|------|
| HBM | All | \pm 2000 | V |
| CDM | All | \pm 500 | V |

Table 23 — EOS Requirement

| Pin | Maximum Rating | Unit | Notes |
|----------|----------------|------|-----------------|
| VIN_BULK | 37 | V | [1],[2],[3],[4] |
| VIN_Mgmt | 10 | V | |

NOTE 1 The test is performed on DDR5 DIMM module without any input capacitor on VIN_BULK and VIN_Mgmt

NOTE 2 The input source needs to follow the waveform and condition as shown in [Figure 11](#) and [Table 24](#).

NOTE 3 Probing is performed at the VIN_BULK and VIN_Mgmt pin of PMIC.

NOTE 4 Each net test is performed individually.

5.4 Absolute Maximum Rating (cont'd)

Table 24 — Input Source Condition

| Item | Value | Notes |
|----------------------------------|----------------------|-------------|
| T (rise from 30% to 90% of peak) | 0.72 μ s (+ 30%) | |
| T1 (rise time) | 1.2 μ s (+ 30%) | T1 = 1.67*T |
| T2 (duration time to half value) | 50 μ s (+ 20%) | |
| Output Impedance | 2 Ω | |
| V _{UNDERSHOOT} Voltage | 30% Max | |

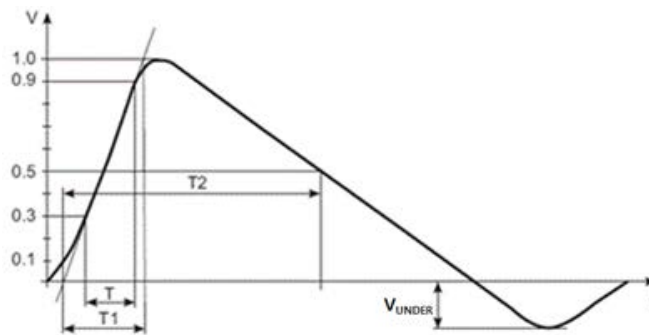


Figure 11 — Impulse Waveform for EOS Test (IEC 61000-4-5)

6 Functional Operation

6.1 PMIC Input Voltage Supplies and Ramp Condition

The DDR5 PMIC has two input supplies from the platform: VIN_Bulk and VIN_Mgmt.

The VIN_Bulk supply is used by the PMIC for all output regulators except for the VOUT_1.8V and VOUT_1.0V LDO outputs regulators when not in switchover mode. The VIN_Bulk input supply may also be used to generate the internal bias voltage in switchover mode. Note that the VOUT_1.8V LDO output is separate and independent from SWD output, which is for the DRAM VPP rail. The VOUT_1.0V LDO output is separate and independent from SWA, SWB, SWC, SWE or SWF.

The PMIC internally generates on its own bias voltage (VBias).

At first power on, the VIN_Bulk input supply shall reach a minimum threshold voltage value per register [Table 131, Register 0x1A \[7:5\]](#) plus 1.0 V offset before it can be detected as a valid input supply to the PMIC. The PMIC filters any non-monotonic noise after this threshold. After power on, with valid VIN_Mgmt input supply while PMIC is operating in non write-protect mode of operation, if VIN_Bulk input supply is removed and re-applied, it must reach the same threshold voltage value per [Table 131, Register 0x1A \[7:5\]](#) plus 1.0 V offset.

The VIN_Mgmt supply shall be used to read out its internal memory content and to supply VOUT_1.8V and VOUT_1.0V to other devices such as SPD, TS and RCD on the DIMM. At first power on, the VIN_Mgmt supply shall reach a minimum of 2.8 V before it can be detected as a valid input supply to the PMIC. At power on, the PMIC floats CAMP signal and then drives CAMP output signal low only when VIN_Mgmt input supply reaches minimum of 2.8 V and PMIC VOUT_1.8V and VOUT_1.0V LDO outputs are valid. VIN_Bulk input supply does not trigger PMIC to drive CAMP output signal low at power on. The VIN_Mgmt supply is strictly a voltage input.

The CAMP output is pulled up to either 1.8 V or 3.3 V on the platform or on the host controller. The CAMP pullup voltage (either 1.8 V or 3.3 V) can be available before or after either VIN_Bulk or VIN_Mgmt is valid and stable. If CAMP pullup voltage is available before VIN_Mgmt or VIN_Bulk is applied, the CAMP signal is high and remains High with no leakage path or damage to the PMIC. When VIN_Mgmt is applied to the PMIC and after VOUT_1.8V and VOUT_1.0V LDO outputs are valid, the PMIC asserts CAMP output low.

[Figure 12](#) and [Figure 13](#) show PMIC power up sequence when power is first applied. The platform can power up VIN_Bulk and VIN_Mgmt supply in any sequence. [Figure 12](#) shows VIN_Mgmt supply ramps up first prior to VIN_Bulk supply. [Figure 13](#) shows VIN_Bulk supply ramps up first prior to VIN_Mgmt supply. The PMIC does not mandate any specific timing relationship between VIN_Bulk and VIN_Mgmt supply.

The PMIC updates register [Table 113, Register 0x08 \[7\]](#) when VIN_Bulk input supply status is valid.

6.2 Power Up Initialization Sequence

During power on, the host shall:

1. Ramp up VIN_Mgmt supply; Ramp up VIN_Bulk supply; (No timing relationship between two supplies)
2. Hold VIN_Mgmt supply stable for a minimum of tVIN_Mgmt_to_Enable time
3. Hold VIN_Bulk supply stable for a minimum of tVIN_Bulk_to_Enable time
4. Query the status of the PMIC status register to determine if it is safe to enable VR.
5. If it is safe to enable, send VR Enable command by setting register [Table 155, Register 0x32 \[7\]](#) = '1' or by issuing DEVCTRL CCC (VR_OE pin must be pulled High via 200 K Ω resistor and [Table 263, Register 0x5F \[5\]](#) = '0') or assert VR_OE high (if [Table 263, Register 0x5F \[5\]](#) = '1').

6.2 Power Up Initialization Sequence (cont'd)

Once the VIN_Mgmt supply is valid and stable, the PMIC shall drive VOUT_1.8V and VOUT_1.0V supply within t1.8V_Ready and t1.0V_Ready time. The PMIC shall enable I²C/I³C Basic bus interface function within tManagement_Ready. The host shall not attempt to access the PMIC's memory registers until tManagement_Ready timing requirement is satisfied. Further the host shall not attempt to issue VR Enable command until tVIN_Mgmt_to_Enable and tVIN_Bulk_to_Enable timing requirement is satisfied. In [Figure 12](#), the PMIC allows access to its memory registers for indefinite period of time as long as VIN_Mgmt input supply is valid and PMIC does not require VIN_Bulk input supply.

The host may read PMIC's own internal memory content prior to ramping VIN_Bulk supply.

The host, prior to issuing VR Enable command, must keep VIN_Mgmt input supply valid as long as VOUT_1.8V and VOUT_1.0V LDO output are required. If VIN_Mgmt input supply is removed or drops below 2.8 V, the PMIC does not guarantee any operation including VOUT_1.8V and VOUT_1.0V LDO output as well as access to its I²C/I³C Basic interface regardless of VIN_Bulk input supply status.

After host issues VR Enable command to the PMIC, the PMIC offers the input supply switchover function. The PMIC has an automatic internal input supply switchover function from VIN_Mgmt input supply to VIN_Bulk input supply. The PMIC triggers the switchover to VIN_Bulk input supply when VIN_Mgmt input supply drops below the threshold set in register [Table 152, Register 0x2F](#) [7]. The internal input supply switchover is for PMIC's VOUT_1.8V and VOUT_1.0V LDO output. The PMIC's I²C/I³C Basic interfaces (SCL/SDA) are kept alive when PMIC switches over to VIN_Bulk input supply. [Figure 14](#) shows automatic internal switchover function when VIN_Mgmt input supply drops below the threshold while maintaining its LDO outputs as well as I²C/I³C Basic interfaces. Under the switchover conditions VIN_Mgmt back-feed voltage shall be less than 0.2 V. While PMIC is in switchover mode to VIN_Bulk, the VIN_Mgmt input supply can re-power backup at any time and PMIC switches back to VIN_Mgmt input supply for its LDO outputs and I²C/I³C interface continues to operate as normal.

The PMIC shall power up its output switch regulators when it registers VR Enable command either via I²C/I³C bus command (VR_OE pin must be pulled High via 200 K Ω resistor and [Table 263, Register 0x5F](#) [5] = '0') or via assertion of VR_OE pin high (if [Table 263, Register 0x5F](#) [5] = '1').

After VR Enable command is registered, the PMIC shall complete the following steps within tPMIC_PWR_GOOD_OUT:

1. Check VIN_Bulk, VIN_Mgmt and VBias Power Good status is valid.
2. Power up itself - PMIC executes Power On Sequence Config 0 to Power On Sequence Config 5 registers and configures PMIC internal registers as programmed in DIMM vendor memory space registers.
3. Power up all enabled output switch regulators and ready for normal operation
4. Update status registers [Table 113, Register 0x08](#) [5:2], [Table 175, Register 0x108](#) [7:6] and float CAMP signal.

If PMIC CAMP signal is not pulled High within tPMIC_PWR_GOOD_OUT time, the host can access the PMIC status registers for detailed information after tPMIC_PWR_GOOD_OUT time. The PMIC may NACK for any host request on I²C or I³C bus after VR Enable command until tPMIC_PWR_GOOD_OUT time expires.

Note that in [Figure 12](#) and [Figure 13](#), the specific sequence of ramping the output regulators (VOUT_A, VOUT_B, VOUT_C and VOUT_D) is for example purpose only. The specific ramp up sequence is configurable through the registers.

Once PMIC's output regulators are running, the PMIC allows VIN_Bulk input supply to vary. [Figure 15](#) shows that VIN_Bulk can go as low as VIN_Bulk Min value (4.25 V) and PMIC output regulators will continue to operate as normal. The VIN_Mgmt input supply can drop and may re-power back up at any time.

6.3 Power Up Sequence

Figure 12 shows the power up initialization sequence.

After VIN_Bulk supply is valid and stable, the PMIC powers up its output regulators when the system host sends VR Enable command either via I²C/I³C bus command (VR_OE pin must be pulled High via 200K Ω resistor and Table 263, Register 0x5F [5] = '0') or via assertion of VR_OE pin high (if Table 263, Register 0x5F [5] = '1'). The PMIC shall generate its bias voltage (VBias) on its own using VIN_Bulk input supply. Further it executes Power On Sequence Config0 to Config5 as configured in register Table 232, Register 0x40 to Table 236, Register 0x44 and Table 265, Register 0x61 to enable its output regulators in the sequence as specified. The PMIC ensures CAMP signal is floated within maximum of tPMIC_PWR_GOOD_OUT after registering VR Enable command.

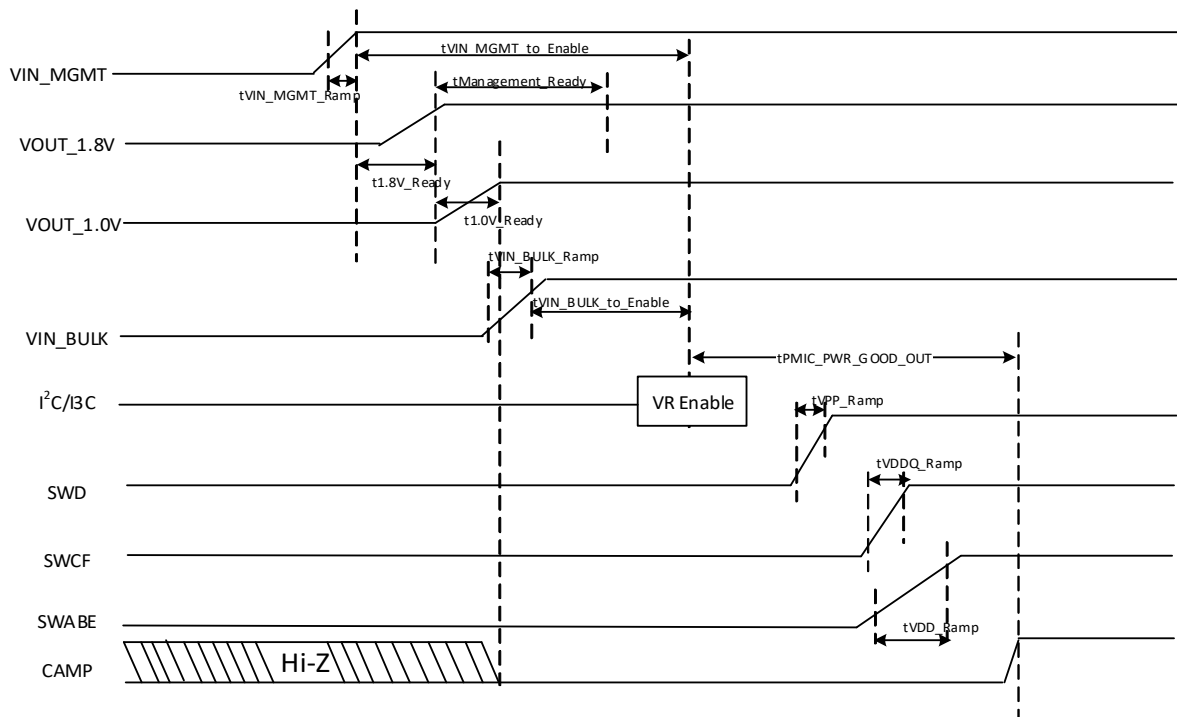


Figure 12 — PMIC Power Up Sequence; VIN_Mgmt followed by VIN_Bulk

6.3 Power Up Sequence (cont'd)

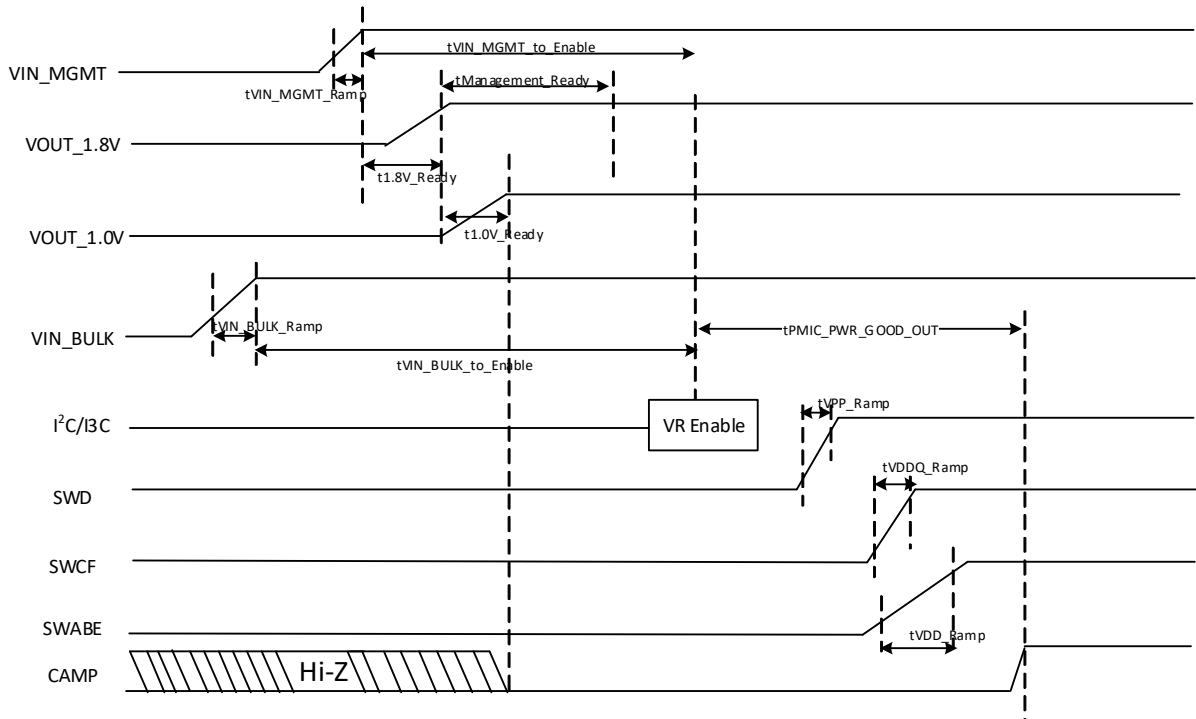


Figure 13 — PMIC Power Up Sequence; VIN_Bulk followed by VIN_Mgmt

6.3 Power Up Sequence (cont'd)

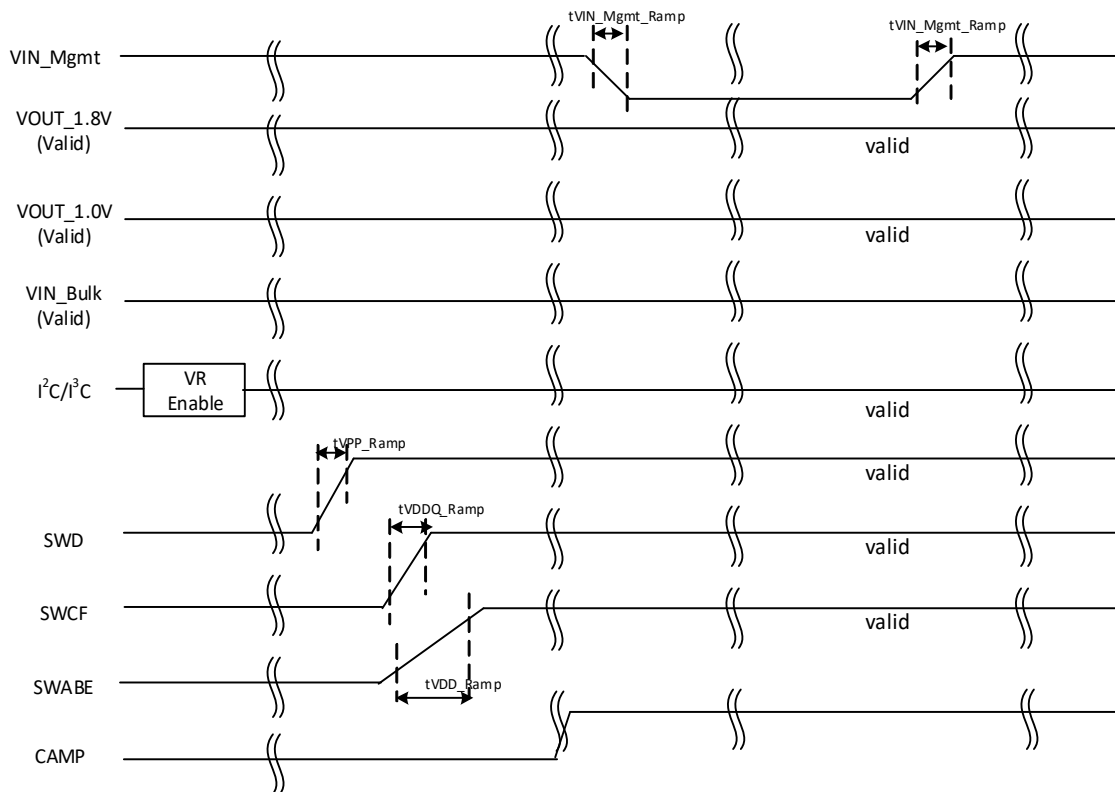


Figure 14 — VIN_Mgmt Input Supply to VIN_Bulk Input Supply Switchover Function

6.3 Power Up Sequence (cont'd)

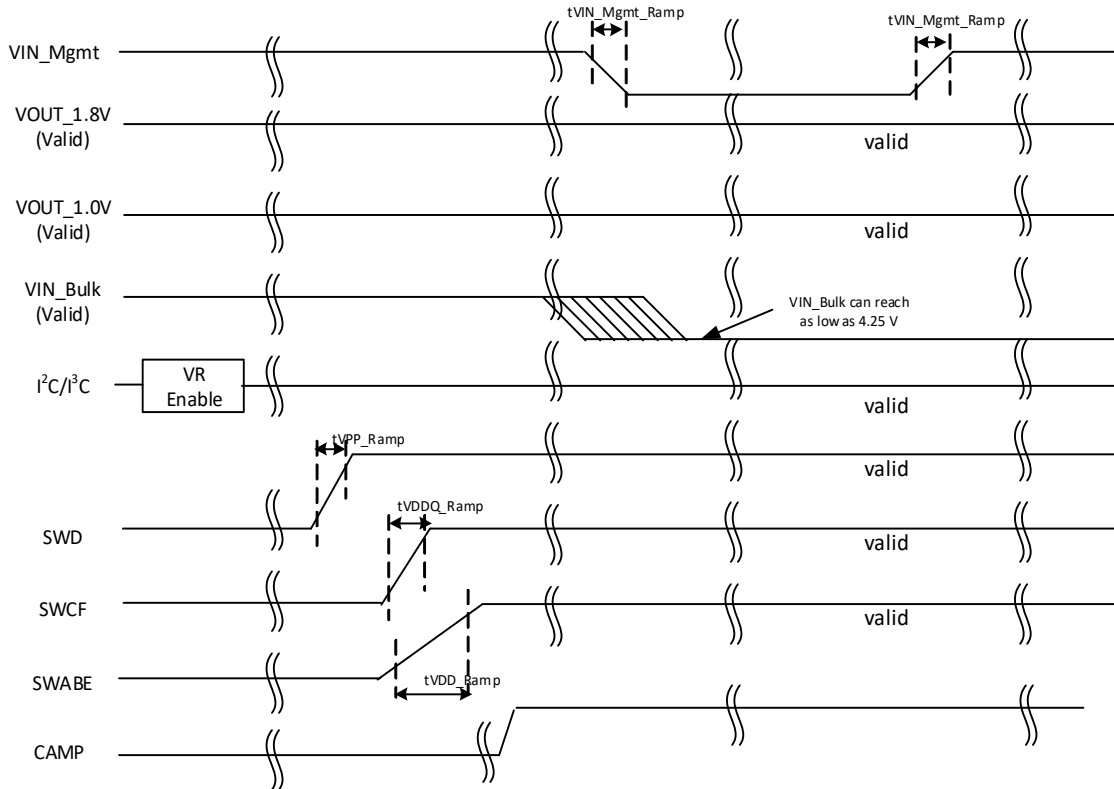


Figure 15 — VIN_Bulk Transition

The timing waveform example in Figure 15 assumes VIN_Bulk threshold is set to 4.25 V in Table 131, Register 0x1A [7:5] and hence CAMP signal remains at valid High level.

6.4 Enabling PMIC Output Switch Voltage Regulators

After first power on, the PMIC automatically enables VOUT_1.8V and VOUT_1.0V LDO output regulators and primary I²C/I³C Basic port based on valid VIN_Mgmt input.

Figure 16 shows the timing relationship once the PMIC receives VR Enable command and when it floats CAMP output signal; timing parameter tPMIC_PWR_GOOD_OUT applies. This timing parameter is a sum of maximum soft start time and configured delay for each power on sequence config registers that are executed plus additional 5 ms timing margin error. The waveform shows each buck regulator output soft start time and delay time once the soft start time expires for each power on sequence config0 to power on sequence config3 registers. Note that if more than one regulators are enabled in a power on sequence config register and if those regulators have different soft start time programmed, then the larger value of that soft start time is used as a reference for delay timer to start. Each regulator will still follow different soft start time to turn on the buck regulator.

The specific example in Figure 16 uses only three power on sequence config0 to config2 registers and only one buck regulator is enabled in power on sequence config 0 register, power on sequence config 1 register and power on sequence config 2 register. The power on sequence config 2 register enables three phase regulator for SWA, SWB and SWE and power on sequence config 1 register enables dual phase regulator for SWC and SWF.

6.4 Enabling PMIC Output Switch Voltage Regulators (cont'd)

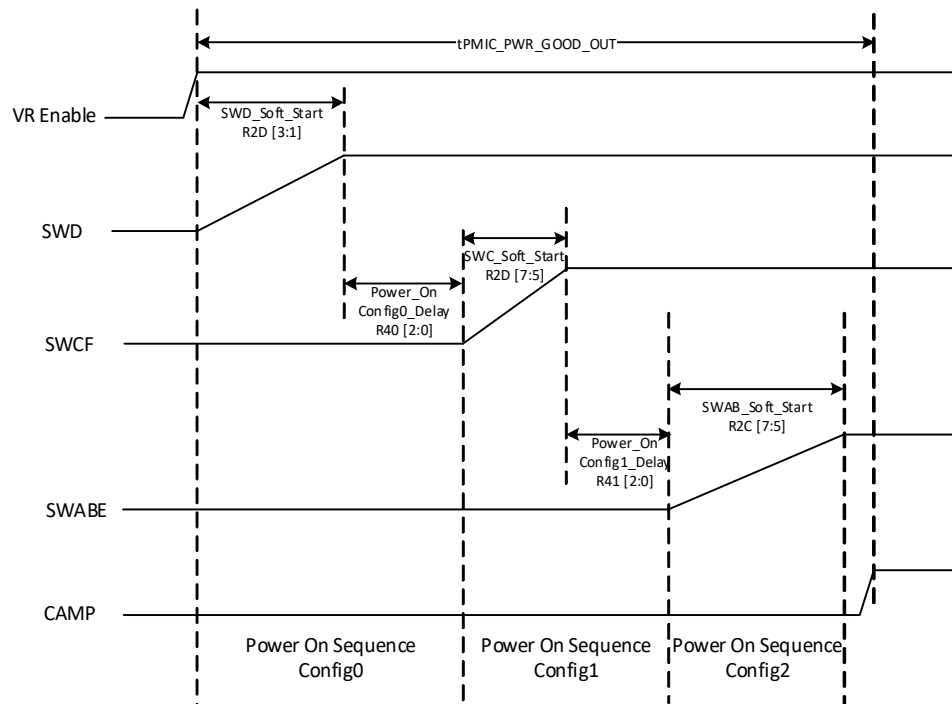


Figure 16 — PMIC Power On Timing

6.5 Auto Power On

The PMIC offers auto power on feature by setting [Table 263, Register 0x5F \[6\] = '1'](#). When this feature is enabled, the PMIC automatically executes the VR Enable command (i.e., [Table 155, Register 0x32 \[7\] = '1'](#)) after both VIN_Bulk and VIN_Mgmt input supplies reach at stable valid levels (VR_OE pin is pulled to High via 200KΩ resistor). The PMIC executes power on sequence configuration registers ([Table 232, Register 0x40](#) to [Table 236, Register 0x44](#) and [Table 265, Register 0x61](#)) and floats CAMP signal.

[Figure 17](#) shows an example of Auto Power on. Once the auto power on is complete, it shows an example of VIN_Bulk fault event followed by re-enabling the output regulators with a VR Enable command on I²C bus once the VIN_Bulk is valid. VR_OE pin is pulled up High to VIN_Bulk on DIMM PCB.

When the [Table 263, Register 0x5F \[6\] = '1'](#) is burned in the DIMM vendor region, the PMIC requires valid stable VIN_Bulk and VIN_Mgmt input supplies. However, first time when this register is burned, the PMIC does not execute the VR Enable command (i.e., [Table 155, Register 0x32 \[7\] = '1'](#)) even though valid VIN_Bulk and VIN_Mgmt input supply is present. The PMIC requires complete power cycle in order to take the effect of burning the [Table 263, Register 0x5F \[6\] = '1'](#).

The PMIC considers the setting of [Table 263, Register 0x5F \[6:5\] = '11'](#) as illegal configuration and the PMIC may not execute Power On Sequence Configuration registers.

6.5 Auto Power On (cont'd)

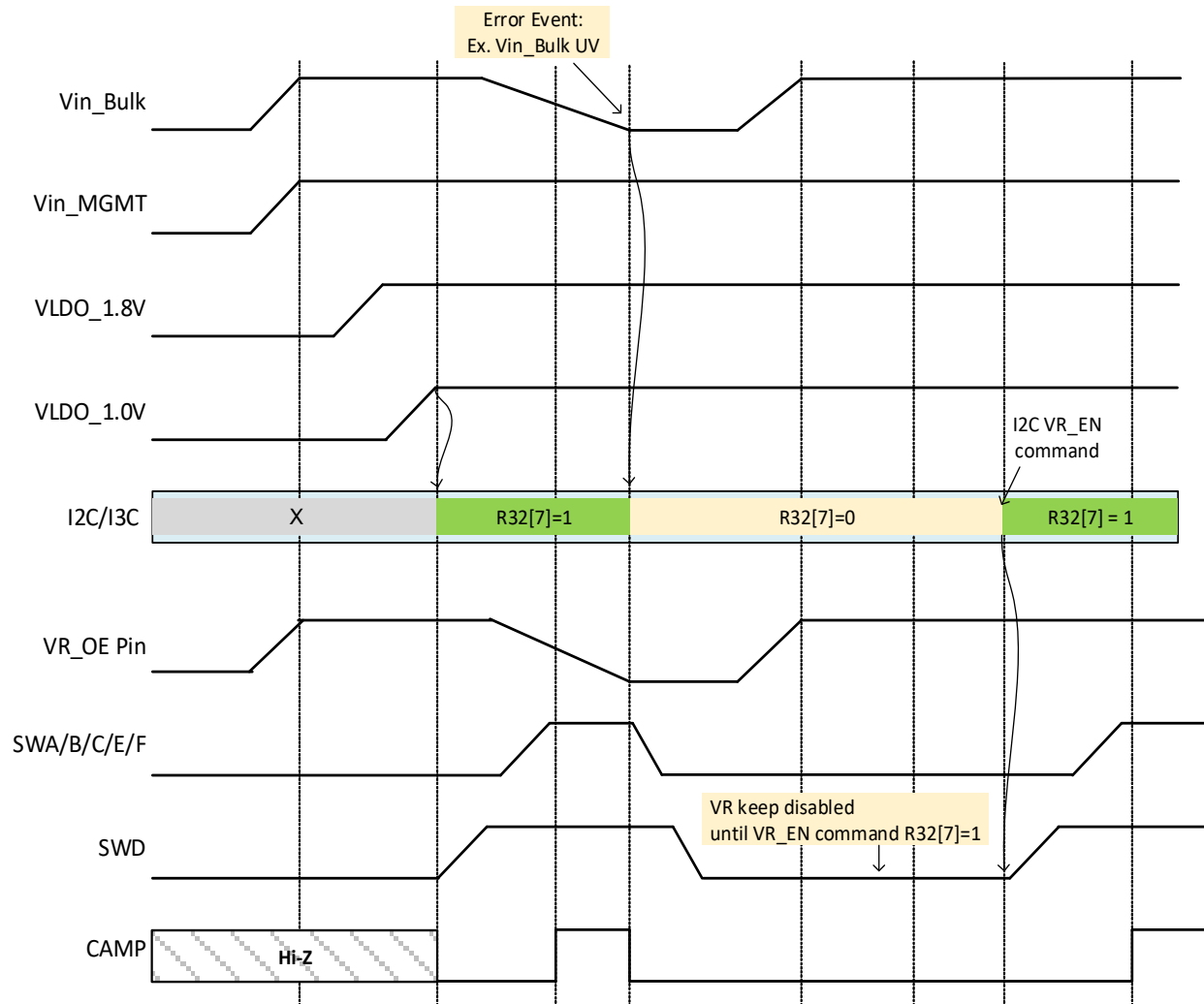


Figure 17 — PMIC Auto Power On Timing

6.6 Power On with VR_OE Pin

The PMIC offers a feature to turn on the output regulators with a dedicated pin by setting [Table 263, Register 0x5F \[5\] = '1'](#). When this feature is enabled VR_OE pin must be held at Low while VIN_Bulk and VIN_Mgmt input supplies are ramping up. When valid stable VIN_Bulk and VIN_Mgmt input supplies are present, the PMIC executes VR Enable command (i.e., [Table 155, Register 0x32 \[7\] = '1'](#)) when VR_OE input pin is asserted to High. The PMIC executes power on sequence configuration registers ([Table 232, Register 0x40](#) to [Table 236, Register 0x44](#) and [Table 265, Register 0x61](#)), floats CAMP signal and enters in write-protect mode if [Table 152, Register 0x2F \[2\] = '0'](#). The VR_OE pin must remain at stable high level for entire power on sequence.

6.6 Power On with VR_OE Pin (cont'd)

The PMIC executes VR Disable command (i.e., [Table 155, Register 0x32 \[7\] = '0'](#)), when VR_OE input pin is de-asserted to Low. The PMIC executes power off sequence configuration registers ([Table 256, Register 0x58](#) to [Table 260, Register 0x5C](#) and [Table 266, Register 0x62](#)), asserts CAMP signal low and PMIC returns to non-write-protect mode. The PMIC executes VR Disable command (i.e., [Table 155, Register 0x32 \[7\] = '0'](#)) even if [Table 263, Register 0x5F \[5\] = '0'](#) when VR_OE input pin is Low. The VR_OE pin must remain at stable low level for entire power off sequence.

When the [Table 263, Register 0x5F \[5\] = '1'](#) is burned in the DIMM vendor region, the PMIC requires valid stable VIN_Bulk and VIN_Mgmt input supplies. However, first time when this register is burned, the VR_OE pin shall be held low. The PMIC requires complete power cycle in order to take the effect of burning the [Table 263, Register 0x5F \[5\] = '1'](#).

The PMIC considers the setting of [Table 263, Register 0x5F \[6:5\] = '11'](#) as illegal configuration; the PMIC may not execute Power On Sequence Configuration registers.

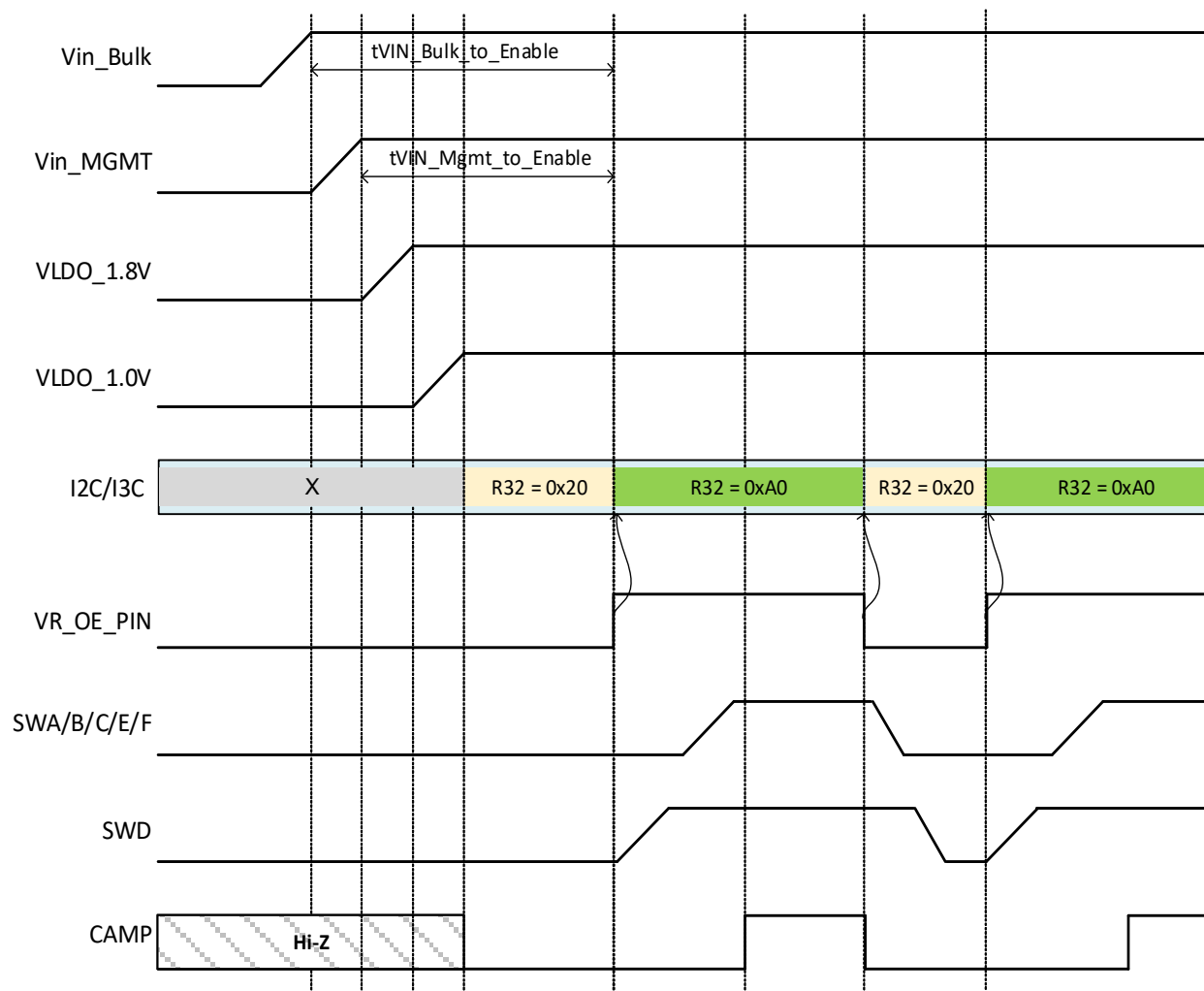


Figure 18 — PMIC Power On with VR_OE Pin

6.7 Combinations to Turn On and Turn Off PMIC Regulators

The PMIC allows to use a combination of VR Enable/Disable command via I²C/I³C bus, VR_OE pin, Auto Power On and CAMP input signal to turn on and turn off output buck regulators. All valid combinations are shown in [Table 25](#).

Table 25 — Valid Combinations to Turn On and Turn Off Regulators

| Register Setting | | | Turn On Regulator Command Method | Turn Off Regulator Command Method |
|------------------|--------|--------|---|--|
| R2F[2] | R5F[6] | R5F[5] | | |
| 0 | 0 | 0 | VR Enable Command (I ² C/I ³ C Write or DEVCTRL CCC) ^[1] | 1. Drive CAMP Input Low 2. Driving VR_OE pin Low ^[2] |
| 1 | 0 | 0 | | 1. Drive CAMP Input Low 2. VR Disable Command (I ² C/I ³ C Write or DEVCTRL CCC) 3. Configure R2F[6:3], R123[1:0] = '0' 4. Driving VR_OE Low ^[1] |
| 0 | 0 | 1 | VR_OE pin Low to High ^[3] | 1. Driving CAMP input Low ^[4] 2. Driving VR_OE pin High to Low |
| 1 | 0 | 1 | | 1. Driving CAMP input Low ^[4] 2. VR Disable Command (I ² C/I ³ C Write or DEVCTRL CCC) ^[4] 3. Configure R2F[6:3], R123[1:0] = '0' ^[4] 4. Driving VR_OE pin High to Low |
| 0 | 1 | 0 | First time, PMIC automatically powers up ^[1] Next time: VR Enable Command (I ² C/I ³ C Write or DEVCTRL CCC) ^[1] | 1. Drive CAMP Input Low 2. Driving VR_OE pin Low ^[1] |
| 1 | 1 | 0 | | 1. Driving CAMP input Low 2. VR Disable Command (I ² C/I ³ C Write or DEVCTRL CCC) 3. Configure R2F[6:3], R123[1:0] = '0' 4. Driving VR_OE pin High to Low |
| X | 1 | 1 | Illegal configuration | Illegal configuration |

NOTE 1 If VR_OE pin is High.

NOTE 2 Assuming that VR_OE pin was High.

NOTE 3 After VR OE pin Low to High, PMIC turns on the regulator. Subsequently, if CAMP input signal is driven low while VR_OE pin is high or if there is an internal fault that triggers VR Disable command, the PMIC turns off the regulator. At this point, PMIC allows VR Enable command via I²C or I³C bus command to turn on the regulators.

NOTE 4 Even if VR_OE pin remains High.

6.8 Power Down Output Regulators

Regardless of how PMIC's output regulators are turned on, the PMIC's output regulators are powered down as described below depending on mode of operation.

6.8.1 Normal Power Down Sequence

Under normal operating condition with valid VIN_Bulk input supply, to disable the PMIC output regulators, the PMIC allows following three methods for normal power down sequence.

- VR_OE pin de-assertion to Low
- VR Disable command on I2C or I3C bus (if PMIC is non-write-protect mode)
- CAMP input from High to Low

All three methods trigger the PMIC to generate internal VR Disable command and the PMIC executes the normal power down sequence as programmed in Power Off Sequence Config0 to Power Off Sequence Config5 registers (Table 256, Register 0x58 to Table 260, Register 0x5C, Table 266, Register 0x62) in DIMM vendor region MTP memory.

The PMIC requires valid VIN_Bulk input supply (i.e., minimum of 4.25 V) to execute normal power down sequence. In a platform where VIN_Bulk input supply ramp down rate is very slow (starting from VIN_Bulk nominal condition of 12 V until it ramps down to 4.25 V), the PMIC may be able to execute normal power down sequence before VIN_Bulk input supply is completely removed depending on the ramp down rate and programmed soft stop time and delay time in Power Off Sequence Config registers. If VIN_Bulk ramp down is very fast (e.g., instantaneous with 0ns), the PMIC cannot execute normal power down sequence to turn off the buck regulators.

Figure 19 shows one example of normal power down sequence where PMIC regulators are turned off by VR Disable command (PMIC is in non-write-protect mode) on I²C bus. The PMIC executes Power Off Sequence Config0 to Power Off Sequence Config3 registers (Table 256, Register 0x58 to Table 259, Register 0x5B). The example shows the power down sequence spread out over four Power Off Sequence Config (0 to 3) registers where only one buck regulator is turned off in each Power Off Sequence Config registers. The sequence shows the order where SWA is turned off first followed by delay, then SWB is turned off followed by delay, then SWC is turned off followed by delay and at last SWD is turned off. Each buck regulator follows its own timing for soft stop time as configured. The example assumes only four buck regulators were turn on in Power On Sequence Config registers.

The PMIC allows any combination where all regulators can be turned off only in first Power Off Sequence Config0 registers or one or more buck regulators are turned off in any given Power Off Sequence Config registers. The PMIC also allows where no buck regulators are turned off in any Power Off Sequence Config to insert additional delay between Power Off Sequence Config registers.

6.8.1 Normal Power Down Sequence (cont'd)

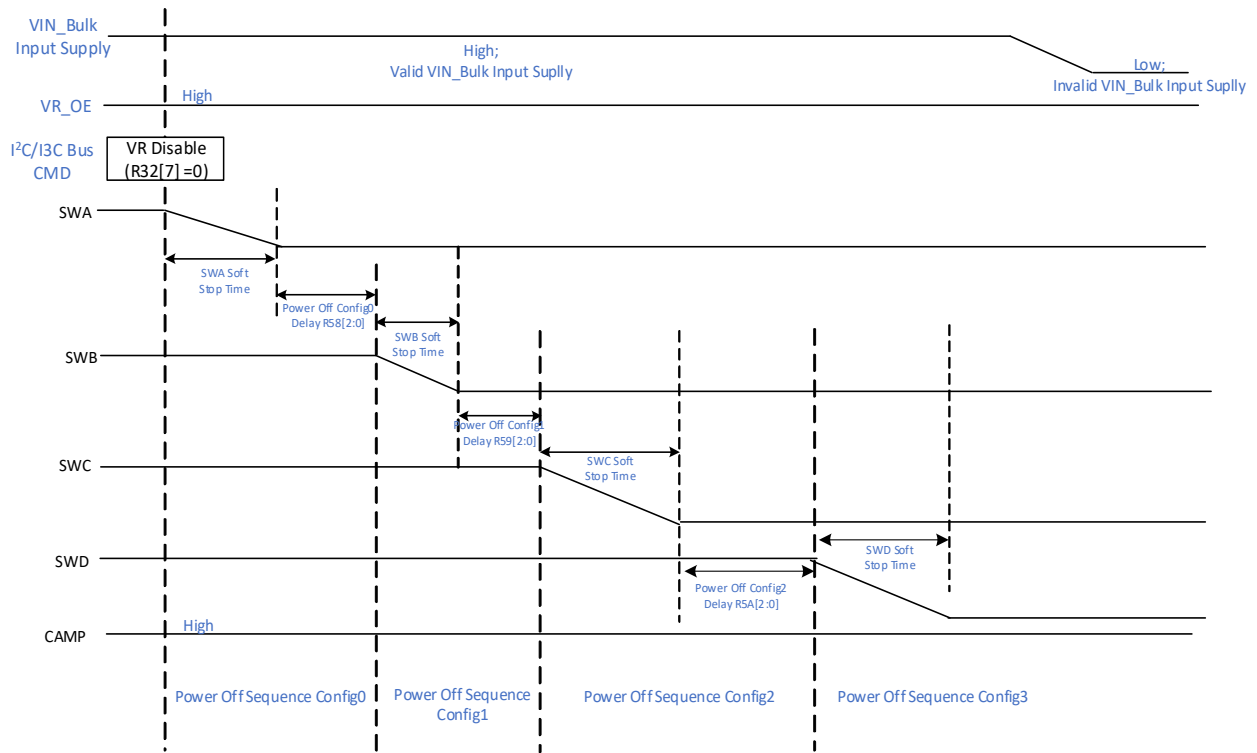


Figure 19 — Normal Power Down Sequence with VR Disable Command

6.8.2 Non Write-Protect Mode - Turning Off Buck Regulators

In non write-protect mode of operation, the PMIC allows host to power off any or all output regulators. The host can disable PMIC's any or all output regulators by any of the four methods below.

1. The VR Disable command (Table 155, Register 0x32 [7] = '0'). The PMIC executes power off sequence config0 to power off sequence config5 (Table 256, Register 0x58 to Table 260, Register 0x5C, Table 266, Register 0x62) to preserve the appropriate voltage relationship as configured by the DIMM vendors. The PMIC keeps the CAMP signal floating (i.e., it remains High) because this is an intentional command from the host and not a fault condition. Note that host can re-enable the PMIC's output regulator by issuing VR Enable command. The PMIC executes power on sequence config 0 to config 5 registers and keeps the CAMP signal floating (i.e., it remains High).
2. Configuring one or more bits in Table 152, Register 0x2F [6:3], Table 191, Register 0x123 [1:0] to '0' in any specific sequence that is desired by the host. The PMIC does not execute power off sequence config0 (Table 256, Register 0x58) to power off sequence config5 (Table 260, Register 0x5C, Table 266, Register 0x62) on its own. The PMIC keeps the CAMP signal floating (i.e., it remains High) because this is intentional command from the host and not a fault condition. Note that host can re-enable any of disabled output regulators by configuring one or more bits in Table 152, Register 0x2F [6:3], Table 191, Register 0x123 [1:0] to '1' in any specific sequence that is desired by the host. The PMIC keeps the CAMP signal floating (i.e., it remains High).

6.8.2 Non Write-Protect Mode - Turning Off Buck Regulators (cont'd)

3. By driving CAMP input low. The PMIC executes power off sequence config0 to power off sequence config5 (Table 256, Register 0x58 to Table 260, Register 0x5C, Table 266, Register 0x62) to preserve the appropriate voltage relationship as configured by the DIMM vendors.
4. By driving VR_OE input low. The PMIC executes power off sequence config0 to power off sequence config5 (Table 256, Register 0x58 to Table 260, Register 0x5C, Table 266, Register 0x62) to preserve the appropriate voltage relationship as configured by the DIMM vendors and asserts CAMP signal Low.

6.8.3 Write-Protect Mode - Turning Off Regulators

In write-protect mode of operation, the host can disable PMIC's all enabled output regulators by any of the three methods below.

1. Power cycle the PMIC.
2. By driving CAMP input low. The PMIC executes power off sequence config0 to power off sequence config5 (Table 256, Register 0x58 to Table 259, Register 0x5B, Table 266, Register 0x62) to preserve the appropriate voltage relationship as configured by the DIMM vendors.
3. By driving VR_OE input low (if Table 263, Register 0x5F [5] = '1'). The PMIC executes power off sequence config0 to power off sequence config5 (Table 256, Register 0x58 to Table 259, Register 0x5B, Table 266, Register 0x62) to preserve the appropriate voltage relationship as configured by the DIMM vendors and asserts CAMP signal Low.

6.8.4 Power Down Output Regulators Due to Fault Condition

Regardless of the either mode of the operation, the PMIC, on its own, can generate VR Disable command at any time due to one or more events listed in Table 27 under column "Trigger VR Disable". The PMIC executes power off sequence config0 to power off sequence config5 (Table 256, Register 0x58 to Table 259, Register 0x5B, Table 266, Register 0x62) to preserve the appropriate voltage relationship as configured by the DIMM vendors and asserts CAMP signal Low. The PMIC may also reset its Vbias LDO regulator.

Figure 20 shows the timing relationship once the PMIC registers VR Disable command internally due to fault. The waveform shows each buck regulator output soft stop time and delay time once the soft stop time expires from each power off sequence config0 to power off sequence config5 registers. Note that if more than one regulators are disabled in a power off sequence config register and if those regulators have different soft stop time programmed, then the larger value of that soft stop time is used as a reference for delay timer to start. Each regulator will still follow different soft stop time to turn off the buck regulator.

The specific example in Figure 20 uses only three power off sequence config0 to config2 registers and only one buck regulator is disabled in power off sequence config 2 register. The power off sequence config 0 register disables three phase regulator for SWA, SWB and SWE and power off sequence config2 register disables dual phase regulator SWC and SWF.

6.8.4 Power Down Output Regulators Due to Fault Condition (cont'd)

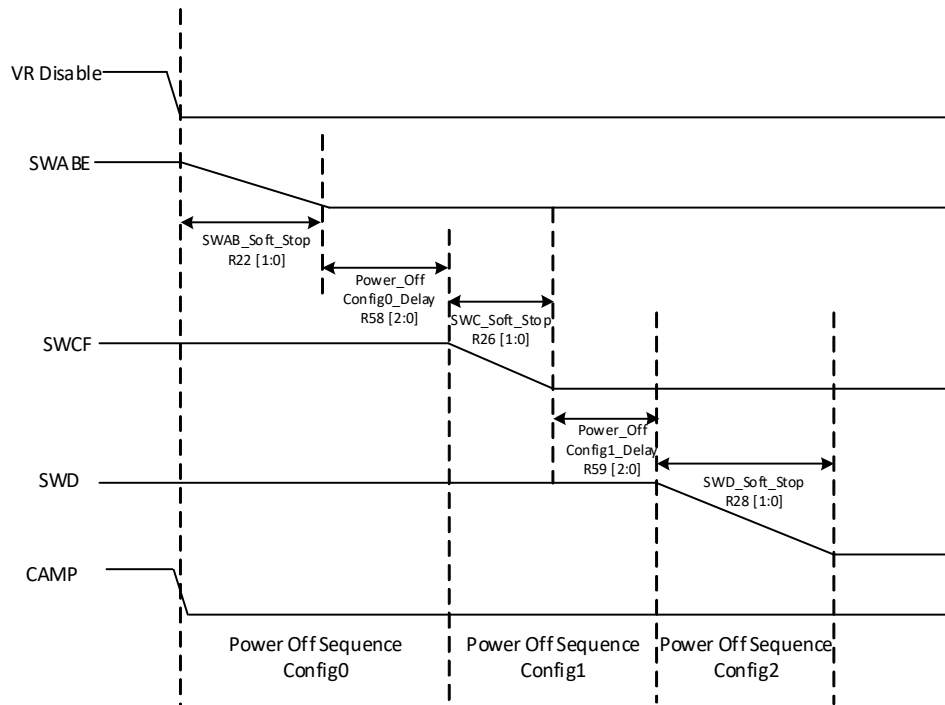


Figure 20 — PMIC Power Off Timing Due to Internal Fault Condition

6.8.5 Power Down Output Regulators During Power On Sequence

During power on as described in clause 6.2 it is possible that PMIC can trigger VR Disable command on its own as described in [Table 27, Events Interrupt Summary](#) when one or more regulators are already turned on even while other remaining output regulators are not yet turned on because PMIC has not completed the power on sequence config registers. For these types of cases, the PMIC will not execute the remaining power on sequence config registers and will immediately jump to executing the power off sequence config0 to power off sequence config5 registers. The PMIC will update the status registers and error log registers appropriately as normal because it generated VR Disable command on its own. The CAMP output signal would remain low.

6.9 CAMP Signal

The CAMP (Control AND Monitor Port) signal provides three different functions.

1. Register write-protect function
2. Fail_n function
3. Status (PWR_GOOD) function

6.9.1 Register Write-Protect Function

The PMIC register write-protect function (i.e., [Table 152, Register 0x2F \[2\]](#)) is configured by the PMIC on its own at first power on based on the [Table 263, Register 0x5F \[7\]](#).

The CAMP input signal level determines when PMIC enters or exits the write-protect mode. The PMIC enters the write-protect mode when CAMP signal is at logic level High and [Table 152, Register 0x2F \[2\]](#) = '0'. PMIC exits the write-protect mode when CAMP signal is at logic level Low. When PMIC is in write-protect mode, the PMIC does not allow to modify registers [Table 126, Register 0x15](#) to [Table 152, Register 0x2F](#), [Table 155, Register 0x32](#), [Table 159, Register 0x35](#) in the host region as well as [Table 232, Register 0x40](#) to [Table 277, Register 0x6F](#) in the DIMM vendor region. These registers are write-protected marked with RED color cells in "Register" column in [Table 107, Host Region - Register Map](#). The PMIC simply ignores the host request for write operation in write-protect mode. PMIC allows all register read access in write-protect mode.

Once PMIC is in write-protect mode, there are 4 ways PMIC can exit write-protect mode:

1. PMIC sees CAMP input signal Low (clause 6.9.2)
2. PMIC triggers internal fault event (VIN_Bulk OV, VIN_Bulk UV, SWx_OV, SWx_UV) and asserts CAMP signal low.
3. PMIC sees VR_OE input signal Low (clause 6.6)
4. PMIC goes through power cycle or power down cycle (i.e., simultaneous removal of VIN_Bulk and VIN_Mgmt input supplies)

If [Table 152, Register 0x2F \[2\]](#) = '1', the PMIC does not enter write-protect mode. The PMIC CAMP input signal has no effect on write-protect function. The PMIC allows write and read access to all registers.

Caution: The operation of non-write-protect mode should be limited to lab and debug environment instead of normal system operation.

6.9.2 Fail_n Function

By default, PMIC Fail_n function is enabled ([Table 155, Register 0x32 \[4\]](#) = '0'). When PMIC CAMP input signal transitions from High to Low, the PMIC executes VR Disable command (i.e., execute power off sequence config0 to config5 registers), asserts CAMP signal low (if [Table 155, Register 0x32 \[3\]](#) = '0'), exits the write-protect mode and clears [Table 155, Register 0x32 \[7\]](#) to '0'.

If [Table 155, Register 0x32 \[4\]](#) = '1', the PMIC Fail_n function is disabled. When CAMP signal transition from High to Low, The PMIC does not execute VR Disable command (i.e., does not execute power off sequence config0 to config5 registers), does not assert CAMP signal low, exits the write-protect mode and does not clear [Table 155, Register 0x32 \[7\]](#) to '0'.

The Fail_n function is independent of PMIC's write-protect function.

6.9.3 Status Function

The PMIC CAMP PWR_GOOD output signal indicates status of VIN_Bulk input supply and all output regulators (VOUT_A, VOUT_B, VOUT_C, VOUT_D, VOUT_E, VOUT_F, VOUT_1.8V, VOUT_1.0V, VBias). Once PMIC receives VR Enable command, the PMIC floats CAMP pin when VIN_Bulk input supply is valid and all enabled output regulator's (VOUT_A, VOUT_B, VOUT_C, VOUT_D, VOUT_E, VOUT_F, VOUT_1.8V, VOUT_1.0V, VBias) tolerances are maintained as configured in the appropriate register space. Note that CAMP pin is not affected based on VIN_Mgmt input supply.

At first power up, with stable and valid input supply VIN_Mgmt as well as VOUT_1.8V and VOUT_1.0V LDO outputs, the PMIC asserts CAMP pin low however PMIC updates corresponding status register. Once PMIC receives VR Enable command from the host, the PMIC enables all appropriate output regulators and updates corresponding status registers and enters state called as "Regulation".

6.9.3 Status Function (cont'd)

At this point, PMIC floats CAMP_PWR_GOOD output and the external board pullup resistor pulls the CAMP pin high. Once the CAMP pin is pulled high (i.e., no other PMIC is driving the CAMP pin low), the PMIC enters state stated called as “online” state.

Once the CAMP pin is high, if PMIC detects any condition either on VIN_Bulk input supply or any of the output regulators (VOUT_A, VOUT_B, VOUT_C, VOUT_D, VOUT_E, VOUT_F, VOUT_1.8V, VOUT_1.0V, VBias) that causes the PMIC to update its status registers to indicate the power status is not good, then PMIC asserts CAMP pin low and keeps it asserted until the host explicitly takes a specific action corresponding to it. The PMIC does not automatically let the CAMP pin float even if the condition that triggered the PMIC to assert the CAMP pin no longer exists. In other words, the PMIC's CAMP pin is latched and once latched, it must be explicitly addressed by the host.

Regardless of whether PMIC is operating in write-protect mode or not, the PMIC always asserts CAMP signal low to indicate the status if there is a fault event.

6.10 GSI_n Signal

General Status Interrupt (GSI_n) is an Open Drain output signal. By default at power on, GSI_n output is disabled. The host can enable the GSI_n output by setting [Table 132, Register 0x1B \[3\] = '1'](#). Typically, GSI_n output is pulled up to 1 K Ω resistor to 1.8 V or 3.3 V. The PMIC asserts GSI_n output for the events as described in [Table 27](#).

6.11 Reset_n Pin Function

PMIC5030 has Reset_n input pin. By default, the Reset_n input pin receiver is disabled at power on. The controller can enable the Reset_n input pin (CMOS input pin receiver) via [Table 192, Register 0x12E \[7:6\]](#).

If Reset_n input pin is enabled, the PMIC resets only the bus interface (I²C or I³C) as if it was a power on reset. The PMIC keeps all output regulators running if they are enabled and there should be no change in PMIC CAMP signal behavior. When Reset_n input pin is asserted, the PMIC always returns to I²C mode ([Table 155, Register 0x32 \[6\] = '0'](#), [Table 153, Register 0x30 \[2\] = '0'](#)), clears the [Table 115, Register 0x0A \[3:2\] = '00'](#), [Table 158, Register 0x34 \[7:5\] = '000'](#) and [Table 158, Register 0x34 \[3:1\] = '111'](#) and floats the SDA signal and clears appropriate state machine if it was previously stuck. The PMIC interface stays in reset as long as Reset_n input pin is asserted. The controller is expected to de-assert the Reset_n input pin followed by SETHID and SETAASA CCC to ensure all components on the module are aligned to same mode of operation. The controller also updates the [Table 153, Register 0x30 \[2\] = '1'](#) for 2 byte address mode. The PMIC ignores any I²C or I³C bus command while Reset_n input is asserted (i.e., PMIC may NACK or may ACK. If PMIC ACKs it, it must return 0x00 data for read and ignore write data).

6.12 State Transition Diagram

Following is a summary of high level description of basic PMIC states.

Offline State:

- VIN_Mgmt is invalid and VIN_Bulk = X (valid or invalid); LDOs are invalid
- All registers are reset to specified default values
- CAMP is Hi-Z

6.12 State Transition Diagram (cont'd)

Configuration (non write-protect) state:

- At initial configuration state, all registers follow the register attributes as defined and read/write accessible.
- The I²C/I³C bus interface is alive and running.
- LDOs are valid; switch regulators are off
- CAMP is low

Regulation (non write-protect) state:

- All registers are read/write accessible.
- All enabled output rails are active
- Internal power good is floated; external CAMP is low

Online (write-protect) state:

- All registers are readable. All non protect registers are writable.
- All enabled output rails are active (i.e., PMIC has registered VR Enable command with [Table 152, Register 0x2F](#) [2] = '0'.
- CAMP is high
- Note: Prior to PMIC registering VR Enable command, PMIC may be configured to not execute VR Enable command and float its CAMP PWR_GOOD output signal ([Table 155, Register 0x32](#) [7:0] = 0x08) with default configuration of [Table 152, Register 0x2F](#) [2] = '0'. In this configuration, PMIC also enters write-protect state when CAMP signal is pulled high.

[Figure 21](#) shows high level simplified state diagram. Specific transition details are function of PMIC's configuration register settings (e.g., R2F, R32, etc., as well as CAMP signal and input/output supplies). Please refer to detail functional description and configuration register definition for PMIC operation. Consider an example of a valid PMIC operation: When the PMIC first powers up from an offline state, the PMIC register [Table 152, Register 0x2F](#) [2] can be configured to '1' followed by VR Enable command. After PMIC turns on all regulators and floats CAMP signal such that it is pulled up High, PMIC is in online state but allows all register write/read access as PMIC is not in write-protect state. In this state, the PMIC does allow to clear [Table 152, Register 0x2F](#) [2] to '0' which will cause PMIC to enter in write-protect state as the CAMP signal was already pulled up High and the PMIC was in regulation.

6.12.1 State Transition with VR_OE Pin

[Table 26](#) shows the high level state transition with using VR OE pin if [Table 263, Register 0x5F](#) [5] = '1'. The table only shows the transition using the VR OE pin to turn on and turn off the regulators along with CAMP signal transition. The PMIC LDOs must be valid to turn on the rails with the VR OE pin. The failure in LDOs returns PMIC in offline state regardless of the VR OE pin level.

6.12.1 State Transition with VR_OE Pin (cont'd)

Table 26 — State Transitions with VR Enable Pin

| Start State | Activity | Register Setting | | | End State | CAMP Output ^[1] | Power Cycle Required? | Note |
|---------------------|---|------------------|--------|--------|-----------------------|----------------------------|-----------------------|------|
| | | R2F[2] | R32[5] | R32[4] | | | | |
| Offline | Valid VIN_Bulk & VIN_Mgmt | N/A | N/A | N/A | Configuration | Low | N/A | |
| Configuration State | VR_OE Pin; Low to High | X | 0 | X | Configuration | Low | No | |
| | | X | 1 | X | Regulation --> Online | Hi-Z | No | [2] |
| Online | VR_OE Pin; High to Low | X | X | X | Configuration | Low | No | [3] |
| Online | CAMP Input; High to Low | X | X | 0 | Configuration | Low | No | [4] |
| | | X | X | 1 | Regulation | Hi-Z | No | [5] |
| | Internal VR Disable Event or VIN_Bulk Invalid | X | X | X | Configuration | Low | No | |
| | Invalid VIN_Bulk & VIN_Mgmt | X | X | X | Offline | Undefined | N/A | |

NOTE 1 This represents PMIC's CAMP output signal.

NOTE 2 The PMIC transitions to regulation state first and then to online state when CAMP signal is pulled up high. The [Table 152, Register 0x2F](#) [2] decides whether PMIC is in write-protect state or non-write-protect state. The PMIC updates the [Table 155, Register 0x32](#) [7] to '1' when it transitions to regulation state.

NOTE 3 The PMIC updates the [Table 155, Register 0x32](#) [7] to '0' when it transitions to configuration state.

NOTE 4 The PMIC returns to non-write-protect configuration state.

NOTE 5 The PMIC returns to non-write-protect regulation state.

6.12.1 State Transition with VR_OE Pin (cont'd)

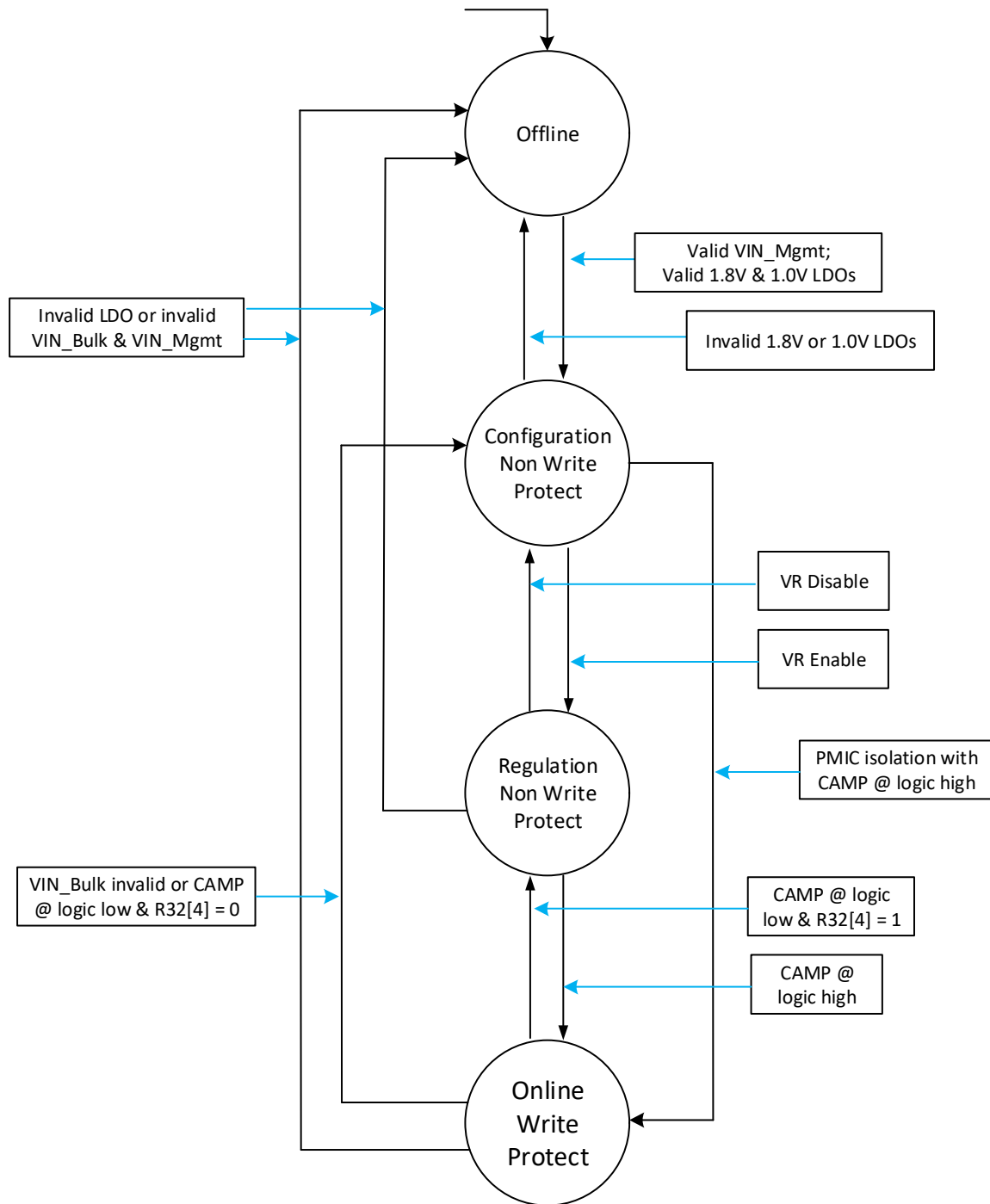


Figure 21 — High Level State Transitions

6.13 Function Interrupt - CAMP and GSI_n Output Signals

This clause defines the output functionality of GSI_n pin and CAMP pin.

When mask register bits are not set, the PMIC asserts its GSI_n output and CAMP output signals as shown in Table 27 when any event occurs. The table also highlights 15 events that cause the PMIC to generate an internal VR Disable command. For remaining events that do not trigger an internal VR Disable command, the PMIC continues to operate as normal.

Table 27 — Events Interrupt Summary

| Event | Status Bit | Clear Bit | Mask Bit | Threshold Bits | Trigger VR Disable? | CAMP Output | GSI_n Output |
|--|------------|-----------|----------|----------------------|---------------------|-------------|--------------|
| VIN_Bulk Power Good | R08 [7] | R10 [7] | R15 [7] | R1A [7:5] | No | Low | Low |
| VIN_Bulk Over Voltage | R08 [0] | R10 [0] | R15 [0] | R1B [7] | Yes | Low | Low |
| VIN_Mgmt Over Voltage | R08 [1] | R10 [1] | R15 [1] | R1B [5] | No | High | Low |
| SWA Output Power Good | R08 [5] | R10 [5] | R15 [5] | R21 [0]; R22 [7:6] | No | Low | Low |
| SWB Output Power Good | R08 [4] | R10 [4] | R15 [4] | R23 [0]; R24 [7:6] | No | Low | Low |
| SWC Output Power Good | R08 [3] | R10 [3] | R15 [3] | R25 [0]; R26 [7:6] | No | Low | Low |
| SWD Output Power Good | R08 [2] | R10 [2] | R15 [2] | R27 [0]; R28 [7:6] | No | Low | Low |
| SWE Output Power Good | R108 [7] | R10E [7] | R114 [7] | R11D [0]; R11E [7:6] | No | Low | Low |
| SWF Output Power Good | R108 [6] | R10E [6] | R114 [6] | R11F [0]; R120 [7:6] | No | Low | Low |
| 1.8 V LDO Power Good | R09 [5] | R11 [5] | R16 [5] | R1A [2] | No | Low | Low |
| 1.0 V LDO Power Good | R33 [2] | R14 [2] | R19 [2] | R1A [0] | No | Low | Low |
| VBias1 or VBias2 LDO Power Good | R09 [6] | R11 [6] | R16 [6] | R1A [3] | No | Low | Low |
| SWA Output Over Voltage | R0A [7] | R12 [7] | R17 [7] | R22 [5:4] | Yes | Low | Low |
| SWB Output Over Voltage | R0A [6] | R12 [6] | R17 [6] | R24 [5:4] | Yes | Low | Low |
| SWC Output Over Voltage | R0A [5] | R12 [5] | R17 [5] | R26 [5:4] | Yes | Low | Low |
| SWD Output Over Voltage | R0A [4] | R12 [4] | R17 [4] | R28 [5:4] | Yes | Low | Low |
| SWE Output Over Voltage | R108 [3] | R10E [3] | R114 [3] | R11E [5:4] | Yes | Low | Low |
| SWF Output Over Voltage | R108 [2] | R10E [2] | R114 [2] | R120 [5:4] | Yes | Low | Low |
| SWA Output Under Voltage | R0B [3] | R13 [3] | R18 [3] | R22 [3:2] | Yes | Low | Low |
| SWB Output Under Voltage | R0B [2] | R13 [2] | R18 [2] | R24 [3:2] | Yes | Low | Low |
| SWC Output Under Voltage | R0B [1] | R13 [1] | R18 [1] | R26 [3:2] | Yes | Low | Low |
| SWD Output Under Voltage | R0B [0] | R13 [0] | R18 [0] | R28 [3:2] | Yes | Low | Low |
| SWE Output Under Voltage | R109 [7] | R10F [7] | R115 [7] | R11E [3:2] | Yes | Low | Low |
| SWF Output Under Voltage | R109 [6] | R10F [6] | R115 [6] | R120 [3:2] | Yes | Low | Low |
| VBias1 or VBias 2 LDO Output or VIN_Bulk Input Under Voltage | R33 [3] | R14 [3] | R19 [3] | Vendor Specific | Yes | Low | Low |
| SWA Output Current Limit | R0B [7] | R13 [7] | R18 [7] | R20 [7:6] | No | High | Low |
| SWB Output Current Limit | R0B [6] | R13 [6] | R18 [6] | R20 [5:4] | No | High | Low |
| SWC Output Current Limit | R0B [5] | R13 [5] | R18 [5] | R20 [3:2] | No | High | Low |
| SWD Output Current Limit | R0B [4] | R13 [4] | R18 [4] | R20 [1:0] | No | High | Low |
| SWE Output Current Limit | R108 [1] | R10E [1] | R114 [1] | R11C [7:6] | No | High | Low |
| SWF Output Current Limit | R108 [0] | R10E [0] | R114 [0] | R11C [5:4] | No | High | Low |

Table 27 — Events Interrupt Summary (cont'd)

| Event | Status Bit | Clear Bit | Mask Bit | Threshold Bits | Trigger VR Disable? | CAMP Output | GSI_n Output |
|------------------------------------|------------|-----------|----------|----------------|---------------------|-------------|--------------|
| SWA Output High Current/Power | R09 [3] | R11 [3] | R16 [3] | R1C [7:0] | No | High | Low |
| SWB Output High Current/Power | R09 [2] | R11 [2] | R16 [2] | R1D [7:0] | No | High | Low |
| SWC Output High Current/Power | R09 [1] | R11 [1] | R16 [1] | R1E [7:0] | No | High | Low |
| SWD Output High Current/Power | R09 [0] | R11 [0] | R16 [0] | R1F [7:0] | No | High | Low |
| SWE Output High Current/Power | R108 [5] | R10E [5] | R114 [5] | R11A [7:0] | No | High | Low |
| SWF Output High Current/Power | R108 [4] | R10E [4] | R114 [4] | R11B [7:0] | No | High | Low |
| High Temperature Warning | R09 [7] | R11 [7] | R16 [7] | R1B [2:0] | No | High | Low |
| Critical Temperature | R08[6] | N/A | N/A | R2E [2:0] | Yes | Low | Low |
| VIN_Mgmt to VIN_Bulk Switchover | R09 [4] | R11 [4] | R16 [4] | R2F [7] | No | High | Low |
| Valid VIN_Mgmt in Switchover State | R33 [4] | R14 [4] | R19 [4] | N/A | No | High | Low |
| PEC Error | R0A [3] | R12 [3] | R17 [3] | N/A | No | High | Low |
| Parity Error | R0A [2] | R12 [2] | R17 [2] | N/A | No | High | Low |

The host is expected to read appropriate status registers to determine and isolate the cause of the GSI_n signal assertion or CAMP signal assertion. The host may attempt to clear or mask the appropriate corresponding interrupt event. The PMIC keeps the GSI_n signal asserted or CAMP signal asserted until the appropriate corresponding registers are explicitly cleared or masked by the host. [Table 28](#) and [Table 29](#) shows the PMIC's response of GSI_n signal and CAMP output signal for each event before and after host issues the Clear command. [Table 28](#) and [Table 29](#) assume that all mask bits are either '0' or '1' for simplicity.

6.13 Function Interrupt - CAMP and GSI_n Output Signals (cont'd)

Table 28 — PMIC Response for Clear Command by Host - 1

| | Event Occurred; All Mask Bits = '0' | | Clear Command; Event Not Present; All Mask Bits = '0' | | Event Occurred; All Mask Bits = '1' | | Clear Command; Event Not Present; All Mask Bits = '1' | |
|--|--|-----------------|---|-----------------|--|-----------------|---|-----------------|
| | | | R2F [1:0] = '00' or '01' or '10' | | R2F [1:0] = '00' | | R2F [1:0] = '00' | |
| Event | CAMP Output | GSI_n Output | CAMP Output | GSI_n Output | CAMP Output | GSI_n Output | CAMP Output | GSI_n Output |
| VIN_Bulk Power Good | Low | Low | High | High | Low | High | High | High |
| VIN_Bulk Over Voltage | Low | Low | Low | High | Low | High | Low | High |
| VIN_Mgmt Over Voltage | High | Low | High | High | High | High | High | High |
| SWA Output Power Good | Low | Low | High | High | Low | High | High | High |
| SWB Output Power Good | Low | Low | High | High | Low | High | High | High |
| SWC Output Power Good | Low | Low | High | High | Low | High | High | High |
| SWD Output Power Good | Low | Low | High | High | Low | High | High | High |
| SWE Output Power Good | Low | Low | High | High | Low | High | High | High |
| SWF Output Power Good | Low | Low | High | High | Low | High | High | High |
| 1.8 V LDO Power Good | Low | Low | High | High | Low | High | High | High |
| 1.0 V LDO Power Good | Low | Low | High | High | Low | High | High | High |
| VBias1or VBias2 LDO Power Good | Low | Low | High | High | Low | High | High | High |
| SWA Output Over Voltage | Low | Low | Low | High | Low | High | Low | High |
| SWB Output Over Voltage | Low | Low | Low | High | Low | High | Low | High |
| SWC Output Over Voltage | Low | Low | Low | High | Low | High | Low | High |
| SWD Output Over Voltage | Low | Low | Low | High | Low | High | Low | High |
| SWE Output Over Voltage | Low | Low | Low | High | Low | High | Low | High |
| SWF Output Over Voltage | Low | Low | Low | High | Low | High | Low | High |
| SWA Output Under Voltage | Low | Low | Low | High | Low | High | Low | High |
| SWB Output Under Voltage | Low | Low | Low | High | Low | High | Low | High |
| SWC Output Under Voltage | Low | Low | Low | High | Low | High | Low | High |
| SWD Output Under Voltage | Low | Low | Low | High | Low | High | Low | High |
| SWE Output Under Voltage | Low | Low | Low | High | Low | High | Low | High |
| SWF Output Under Voltage | Low | Low | Low | High | Low | High | Low | High |
| VBias1 or VBias2 LDO Output or VIN_Bulk Input Under Voltage | Low | Low | Low | High | Low | High | Low | High |
| SWA Output Current Limit | High | Low | High | High | High | High | High | High |
| SWB Output Current Limit | High | Low | High | High | High | High | High | High |
| SWC Output Current Limit | High | Low | High | High | High | High | High | High |
| SWD Output Current Limit | High | Low | High | High | High | High | High | High |
| SWE Output Current Limit | High | Low | High | High | High | High | High | High |
| SWF Output Current Limit | High | Low | High | High | High | High | High | High |

Table 28 — PMIC Response for Clear Command by Host - 1 (cont'd)

| | Event Occurred; All Mask Bits = '0' | | Clear Command; Event Not Present; All Mask Bits = '0' | | Event Occurred; All Mask Bits = '1' | | Clear Command; Event Not Present; All Mask Bits = '1' | |
|---------------------------------|--|-----------------|---|--------------------|--|-----------------|---|--------------------|
| | | | R2F [1:0] = '00' or '01' or '10' | | R2F [1:0] = '00' | | R2F [1:0] = '00' | |
| Event | CAMP Output | GSI_n Output | CAMP Output | GSI_n Output | CAMP Output | GSI_n Output | CAMP Output | GSI_n Output |
| SWA Output High Current/Power | High | Low | High | High | High | High | High | High |
| SWB Output High Current/Power | High | Low | High | High | High | High | High | High |
| SWC Output High Current/Power | High | Low | High | High | High | High | High | High |
| SWD Output High Current/Power | High | Low | High | High | High | High | High | High |
| SWE Output High Current/Power | High | Low | High | High | High | High | High | High |
| SWF Output High Current/Power | High | Low | High | High | High | High | High | High |
| High Temperature Warning | High | Low | High | High | High | High | High | High |
| Critical Temperature | Low | Low | P/C ^[1] | P/C ^[1] | Low | Low | P/C ^[1] | P/C ^[1] |
| VIN_Mgmt to VIN_Bulk Switchover | High | Low | High | High | High | High | High | High |
| Valid VIN_Mgmt in Switchover | High | Low | High | High | High | High | High | High |
| PEC Error | High | Low | High | High | High | High | High | High |
| Parity Error | High | Low | High | High | High | High | High | High |

NOTE 1 P/C = Power Cycle

Table 29 — PMIC Response for Clear Command by Host - 2

| | Event Occurred; All Mask Bits = '1' | | Clear Command; Event Not Present; All Mask Bits = '1' | | Event Occurred; All Mask Bits = '1' | | Clear Command; Event Not Present; All Mask Bits = '1' | |
|---------------------------------|--|-----------------|---|-----------------|--|-----------------|---|-----------------|
| | R2F [1:0] = '01' | | R2F [1:0] = '01' | | R2F [1:0] = '10' | | R2F [1:0] = '10' | |
| Event | CAMP Output | GSI_n Output | CAMP Output | GSI_n Output | CAMP Output | GSI_n Output | CAMP Output | GSI_n Output |
| VIN_Bulk Power Good | High | Low | High | High | High | High | High | High |
| VIN_Bulk Over Voltage | Low | Low | Low | High | Low | High | Low | High |
| VIN_Mgmt Over Voltage | High | Low | High | High | High | High | High | High |
| SWA Output Power Good | High | Low | High | High | High | High | High | High |
| SWB Output Power Good | High | Low | High | High | High | High | High | High |
| SWC Output Power Good | High | Low | High | High | High | High | High | High |
| SWD Output Power Good | High | Low | High | High | High | High | High | High |
| SWE Output Power Good | High | Low | High | High | High | High | High | High |
| SWF Output Power Good | High | Low | High | High | High | High | High | High |
| 1.8 V LDO Power Good | High | Low | High | High | High | High | High | High |
| 1.0 V LDO Power Good | High | Low | High | High | High | High | High | High |
| VBias1 or VBias2 LDO Power Good | High | Low | High | High | High | High | High | High |

Table 29 — PMIC Response for Clear Command by Host - 2 (cont'd)

| | Event Occurred; All Mask Bits = '1' | | Clear Command; Event Not Present; All Mask Bits = '1' | | Event Occurred; All Mask Bits = '1' | | Clear Command; Event Not Present; All Mask Bits = '1' | |
|--|--|-----------------|---|-----------------|--|-----------------|---|-----------------|
| | R2F [1:0] = '01' | | R2F [1:0] = '01' | | R2F [1:0] = '10' | | R2F [1:0] = '10' | |
| Event | CAMP Output | GSI_n Output | CAMP Output | GSI_n Output | CAMP Output | GSI_n Output | CAMP Output | GSI_n Output |
| SWA Output Over Voltage | Low | Low | Low | High | Low | High | Low | High |
| SWB Output Over Voltage | Low | Low | Low | High | Low | High | Low | High |
| SWC Output Over Voltage | Low | Low | Low | High | Low | High | Low | High |
| SWD Output Over Voltage | Low | Low | Low | High | Low | High | Low | High |
| SWE Output Over Voltage | Low | Low | Low | High | Low | High | Low | High |
| SWF Output Over Voltage | Low | Low | Low | High | Low | High | Low | High |
| SWA Output Under Voltage | Low | Low | Low | High | Low | High | Low | High |
| SWB Output Under Voltage | Low | Low | Low | High | Low | High | Low | High |
| SWC Output Under Voltage | Low | Low | Low | High | Low | High | Low | High |
| SWD Output Under Voltage | Low | Low | Low | High | Low | High | Low | High |
| SWE Output Under Voltage | Low | Low | Low | High | Low | High | Low | High |
| SWF Output Under Voltage | Low | Low | Low | High | Low | High | Low | High |
| VBias1 or VBias2 LDO Output or VIN_Bulk Input Under Voltage | Low | Low | Low | High | Low | High | Low | High |
| SWA Output Current Limit | High | Low | High | High | High | High | High | High |
| SWB Output Current Limit | High | Low | High | High | High | High | High | High |
| SWC Output Current Limit | High | Low | High | High | High | High | High | High |
| SWD Output Current Limit | High | Low | High | High | High | High | High | High |
| SWE Output Current Limit | High | Low | High | High | High | High | High | High |
| SWF Output Current Limit | High | Low | High | High | High | High | High | High |
| SWA Output High Current/Power | High | Low | High | High | High | High | High | High |
| SWB Output High Current/Power | High | Low | High | High | High | High | High | High |
| SWC Output High Current/Power | High | Low | High | High | High | High | High | High |
| SWD Output High Current/Power | High | Low | High | High | High | High | High | High |
| SWE Output High Current/Power | High | Low | High | High | High | High | High | High |
| SWF Output High Current/Power | High | Low | High | High | High | High | High | High |
| High Temperature Warning | High | Low | High | High | High | High | High | High |
| Critical Temperature | Low | Low | P/C[1] | P/C[1] | Low | Low | P/C[1] | P/C[1] |
| VIN_Mgmt to VIN_Bulk Switchover | High | Low | High | High | High | High | High | High |
| Valid VIN_Mgmt in Switchover | High | Low | High | High | High | High | High | High |
| PEC Error | High | Low | High | High | High | High | High | High |
| Parity Error | High | Low | High | High | High | High | High | High |

NOTE 1 P/C = Power Cycle

Note that when host masks any of the event in appropriate register, it only masks the assertion of GSI_n output signal or assertion of CAMP output signal for events that do not trigger VR Disable command by the PMIC on its own. The PMIC functional behavior remains the same as noted for each event other than assertion of GSI_n output signal and assertion of CAMP output signal. For any events that cause the PMIC to trigger VR Disable command on its own, the mask register does not apply to CAMP signal and it is always asserted; the mask register does apply to GSI_n signal.

6.14 Input Power Good Status

There is one possibility where PMIC recognizes the input supply fail.

1. VIN_Bulk goes below the threshold set in register [Table 131, Register 0x1A](#) [7:5].

When this event occurs for a period longer than `tInput_PWR_GOOD_GSI_Assertion` time then PMIC sets the register [Table 113, Register 0x08](#) [7] and drives GSI_n and CAMP output signal as shown in [Table 27](#) at the same time. The PMIC continues to operate as normal as long as VIN_Bulk input remains above 4.25 V. See also clause 6.18. The host is responsible for taking any specific action. The host may clear the VIN_Bulk input power good status register by writing '1' to register [Table 121, Register 0x10](#) [7] or by writing '1' to global status clear register [Table 125, Register 0x14](#) [0]. If the input power not good condition is still present then PMIC will continue to drive GSI_n and CAMP output signal as in [Table 27](#) and the status register [Table 113, Register 0x08](#) [7] will remain at '1'. If the input power not good condition persists, the host may set the appropriate mask register to remove GSI_n or CAMP output signal as shown in [Table 28](#) and [Table 29](#).

Note that after VR enable command, when VIN_Mgmt input goes below the threshold set in register [Table 152, Register 0x2F](#) [7], it is reported as switchover event as described in clause 6.23. Prior to VR Enable command, the VIN_Mgmt is always required to be above 2.8 V to guarantee PMIC's functionality as described in clause 6.2.

6.15 Input Over Voltage Protection

An input over voltage protection mechanism is implemented to limit the voltages to the PMIC. The PMIC actively monitors the input voltage VIN_Bulk and VIN_Mgmt rail.

There are two possibilities where PMIC recognizes the input over voltage event.

1. VIN_Mgmt input goes above the threshold set in register [Table 132, Register 0x1B](#) [5].
2. VIN_Bulk input goes above the threshold set in register [Table 132, Register 0x1B](#) [7].

When either one or both event occurs for a period longer than `tInput_OV_GSI_Assertion` time then PMIC sets the register [Table 113, Register 0x08](#) [1:0] accordingly and drives GSI_n output signal as shown in [Table 27](#) at the same time. Note that at this point in time ($< t_{\text{Input_OV_VR_Disable}}$), the PMIC does not assert CAMP output signal. The PMIC continues to operate as normal. The host is responsible for taking any specific action. The host may clear the VIN_Mgmt or VIN_Bulk input over voltage status register by writing '1' to register [Table 121, Register 0x10](#) [1:0] appropriately or by writing '1' to global status clear register [Table 125, Register 0x14](#) [0]. If the input over voltage condition is still present then PMIC will continue to assert GSI_n output signal and the status register [Table 113, Register 0x08](#) [1:0] will remain at '1'.

In non write-protect mode, if VIN_Bulk input supply over voltage condition persists greater than `tInput_OV_VR_Disable` time then PMIC internally generates VR Disable command and disables all of its switching output regulators and asserts CAMP signal. The PMIC keeps its VOUT_1.8V and VOUT_1.0V LDO output regulators active. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the CAMP signal assertion and GSI_n signal assertion. Once host determines the cause, the host must first clear the VIN_Bulk input over voltage status register as well as any other relevant status registers individually or by writing '1' to global status clear register [Table 125, Register 0x14](#) [0] which triggers the GSI_n signal to be de-asserted. If the input over voltage condition is still present then PMIC will continue to assert GSI_n output signal and the status register [Table 113, Register 0x08](#) [0] will remain at '1'. Once the status register is cleared and GSI_n output signal is de-asserted, the host may re-enable the PMIC's output switching regulator by issuing VR Enable command. The PMIC enables output switching regulators and ensures CAMP signal is floated when all of its output regulators are normal and input over voltage condition is no longer present.

6.15 Input Over Voltage Protection (cont'd)

In write-protect mode, if VIN_Bulk input supply over voltage condition persists greater than tInput_OV_VR_Disable time then PMIC internally generates VR Disable command and disables all of its switching output regulators by executing Power Off Sequence configuration registers, asserts CAMP signal low and returns to configuration mode. The PMIC keeps its VOUT_1.8V and VOUT_1.0V LDO output regulators active.

6.16 Output Power Good Status

The PMIC provides the voltage tolerance information to host that its output regulator may have crossed the desired voltage tolerance from its nominal programmed setting. The nominal programmed setting for output regulator SWA, SWB, SWC, SWD, SWE and SWF is programmed in register [Table 138, Register 0x21 \[7:1\]](#), [Table 140, Register 0x23 \[7:1\]](#), [Table 142, Register 0x25 \[7:1\]](#), [Table 144, Register 0x27 \[7:1\]](#), [Table 185, Register 0x11D \[7:1\]](#) and [Table 187, Register 0x11F \[7:1\]](#) respectively. The PMIC offers the CAMP condition to be set independently for low side and high side.

In addition, PMIC has three LDO regulators: VBias, VOUT_1.8V and VOUT_1.0V

There are five possibilities where PMIC recognizes the output power good event for any output regulator.

1. Output voltage goes below the threshold set in register [Table 138, Register 0x21 \[0\]](#) for SWA or [Table 140, Register 0x23 \[0\]](#) for SWB or [Table 142, Register 0x25 \[0\]](#) for SWC or [Table 144, Register 0x27 \[0\]](#) for SWD or [Table 185, Register 0x11D \[0\]](#) for SWE or [Table 187, Register 0x11F \[0\]](#) for SWF.
2. Output voltage goes above the threshold set in register [Table 139, Register 0x22 \[7:6\]](#) for SWA or [Table 141, Register 0x24 \[7:6\]](#) for SWB or [Table 143, Register 0x26 \[7:6\]](#) for SWC or [Table 145, Register 0x28 \[7:6\]](#) for SWD or [Table 186, Register 0x11E \[7:6\]](#) for SWE or [Table 188, Register 0x120 \[7:6\]](#) for SWF.
3. LDO output VBias goes below the threshold set in register [Table 131, Register 0x1A \[3\]](#).
4. LDO output VOUT_1.8V goes below the threshold set in register [Table 131, Register 0x1A \[2\]](#).
5. LDO output VOUT_1.0V goes below the threshold set in register [Table 131, Register 0x1A \[0\]](#).

When either event occurs for a period longer than tOutput_PWR_GOOD_GSI_Assertion time then PMIC sets the register [Table 113, Register 0x08 \[5:2\]](#) or [Table 175, Register 0x108 \[7:6\]](#) or [Table 114, Register 0x09 \[6:5\]](#) or [Table 157, Register 0x33 \[2\]](#) appropriately and drives CAMP and GSI_n output signal as shown in [Table 27](#) at the same time. The PMIC may continue to operate but DDR5 DIMM functionality may not be guaranteed. The host is responsible for taking any specific action. The host may query the PMIC register space to determine and identify the cause of the CAMP signal assertion and GSI_n signal assertion. Once host determines the cause, the host may clear the appropriate status register individually or by writing '1' to global status clear register [Table 125, Register 0x14 \[0\]](#) which triggers the GSI_n signal to be de-asserted and CAMP signal to be de-asserted. If the output power not good condition is still present then PMIC will continue to assert GSI_n output signal and assert CAMP signal and the appropriate status register [Table 113, Register 0x08 \[5:2\]](#) or [Table 175, Register 0x108 \[7:6\]](#) or [Table 114, Register 0x09 \[6:5\]](#) or [Table 157, Register 0x33 \[2\]](#) will remain at '1'. If the output power not good condition persists, the host may set the appropriate mask register to remove GSI_n or CAMP output signal as shown in [Table 28](#) and [Table 29](#).

6.17 Output Over Voltage Protection

An output over voltage protection mechanism is implemented to limit the voltages on the PMIC output regulators. The PMIC actively monitors the output voltage on each enabled regulators.

There are six possibilities where PMIC recognizes the over voltage event.

1. SWA output regulator goes above the threshold set in register [Table 139, Register 0x22](#) [5:4].
2. SWB output regulator goes above the threshold set in register [Table 141, Register 0x24](#) [5:4].
3. SWC output regulator goes above the threshold set in register [Table 143, Register 0x26](#) [5:4].
4. SWD output regulator goes above the threshold set in register [Table 145, Register 0x28](#) [5:4].
5. SWE output regulator goes above the threshold set in register [Table 186, Register 0x11E](#) [5:4].
6. SWF output regulator goes above the threshold set in register [Table 188, Register 0x120](#) [5:4].

In non write-protect mode, if any output over voltage condition persists greater than $t_{Output_OV_VR_Disable}$ time then PMIC internally generates VR Disable command and disables all of its switching output regulators, sets register [Table 115, Register 0x0A](#) [7:4], [Table 175, Register 0x108](#) [3:2] appropriately, asserts CAMP and asserts GSI_n output signal. The PMIC keeps its VOUT_1.8V and VOUT_1.0V LDO output regulators active. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the CAMP signal assertion and GSI_n signal assertion. Once host determines the cause, the host must first clear the appropriate output over voltage status register as well as any other relevant status registers individually or by writing '1' to global status clear register [Table 125, Register 0x14](#) [0] which triggers the GSI_n signal to be de-asserted. Once the status register is cleared and GSI_n output signal is de-asserted, the host may re-enable the PMIC's output switching regulator by issuing VR Enable command. The PMIC enables output switching regulators and ensures CAMP signal is floated when all of its output regulators are normal.

In write-protect mode, if any output over voltage condition persists greater than $t_{Output_OV_VR_Disable}$ time then PMIC internally generates VR Disable command and disables all of its switching output regulators by executing Power Off Sequence configuration registers, asserts CAMP signal low and returns to configuration mode. The PMIC keeps its VOUT_1.8V and VOUT_1.0V LDO output regulators active.

6.18 Output Under Voltage and VIN_Bulk Under Voltage Lockout Protection

An output under voltage lockout protection mechanism is implemented to limit the voltages on the PMIC output regulators. The PMIC actively monitors the output voltage on each enabled regulators. The PMIC also implements the VIN_Bulk under voltage and VBIAS under voltage lockout protection mechanism to limit the voltages.

There are seven possibilities where PMIC recognizes the under voltage lockout event.

1. SWA output regulator goes below the threshold set in register [Table 139, Register 0x22](#) [3:2].
2. SWB output regulator goes below the threshold set in register [Table 141, Register 0x24](#) [3:2].
3. SWC output regulator goes below the threshold set in register [Table 143, Register 0x26](#) [3:2].
4. SWD output regulator goes below the threshold set in register [Table 145, Register 0x28](#) [3:2].
5. SWE output regulator goes below the threshold set in register [Table 186, Register 0x11E](#) [3:2].
6. SWF output regulator goes below the threshold set in register [Table 188, Register 0x120](#) [3:2].
7. VBias LDO output regulator goes below the vendor specific threshold or VIN_Bulk Input Voltage goes below vendor specific threshold.

6.18 Output Under Voltage and VIN_Bulk Under Voltage Lockout Protection (cont'd)

In non write-protect mode, if any output under voltage condition or VIN_Bulk input voltage condition as listed above persists greater than tOutput_UV_VR_Disable time then PMIC internally generates VR Disable command and disables all of its switching output regulators, sets register [Table 116, Register 0x0B \[3:0\]](#), [Table 176, Register 0x109 \[7:6\]](#), [Table 157, Register 0x33 \[3\]](#) appropriately, asserts CAMP and asserts GSI_n output signal. The PMIC keeps its VOUT_1.8V and VOUT_1.0V LDO output regulators active. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the CAMP signal assertion and GSI_n signal assertion. Once host determines the cause, the host must first clear the appropriate output under voltage status register as well as any other relevant status registers individually or by writing '1' to global status clear register [Table 125, Register 0x14 \[0\]](#) which triggers the GSI_n signal to be de-asserted. Once the status register is cleared and GSI_n output signal is de-asserted, the host may re-enable the PMIC's output switching regulator by issuing VR Enable command assuming valid VIN_Bulk input voltage. The PMIC enables output switching regulators and floats CAMP signal when all of its output regulators are normal.

In write-protect mode, if any output under voltage condition or VIN_Bulk input voltage condition as listed above persists greater than tOutput_UV_VR_Disable time then PMIC internally generates VR Disable command and disables all of its switching output regulators by executing Power Off Sequence configuration registers, asserts CAMP signal low and returns to configuration mode. The PMIC keeps its VOUT_1.8V and VOUT_1.0V LDO output regulators active.

6.19 Output Current Limiter Warning Event

The PMIC has output current limiter mechanism to limit the current on the PMIC output voltage regulators. There are six possibilities where PMIC recognizes the current limiter event.

1. SWA output regulator current goes above the threshold set in register [Table 137, Register 0x20 \[7:6\]](#).
2. SWB output regulator current goes above the threshold set in register [Table 137, Register 0x20 \[5:4\]](#).
3. SWC output regulator current goes above the threshold set in register [Table 137, Register 0x20 \[3:2\]](#).
4. SWD output regulator current goes above the threshold set in register [Table 137, Register 0x20 \[1:0\]](#).
5. SWE output regulator current goes above the threshold set in register [Table 184, Register 0x11C \[7:6\]](#).
6. SWF output regulator current goes above the threshold set in register [Table 184, Register 0x11C \[5:4\]](#).

When either event occurs for a period longer than tOutput_Current_Limiter time then PMIC sets the register [Table 116, Register 0x0B \[7:4\]](#), [Table 175, Register 0x108 \[1:0\]](#) appropriately, drives GSI_n output signal as shown in [Table 27](#) at the same time. The PMIC continues to operate as normal. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the GSI_n signal assertion. Once host determine the cause, the host may clear the appropriate output current limiter status register as well as any other status registers individually or by writing '1' to global status clear register in [Table 125, Register 0x14 \[0\]](#) which triggers the GSI_n signal to be de-asserted. If the output current limiter condition is still present then PMIC will continue to assert GSI_n output signal and the appropriate status register in [Table 116, Register 0x0B \[7:4\]](#), [Table 175, Register 0x108 \[1:0\]](#) will remain at '1'. If the output current limiter condition persists, the host may set the appropriate mask register to remove the GSI_n output signal as shown in [Table 28](#) and [Table 29](#).

6.20 Output High Current Consumption Warning Event

The PMIC supports high output current consumption warning mechanism for each of its regulator output. If enabled, the PMIC actively monitors the average output current of the regulator.

There are six possibilities where PMIC recognizes the high output current consumption.

1. SWA output regulator average current goes above the threshold set in register [Table 133, Register 0x1C](#) [7:0].
2. SWB output regulator average current goes above the threshold set in register [Table 134, Register 0x1D](#) [7:0].
3. SWC output regulator average current goes above the threshold set in register [Table 135, Register 0x1E](#) [7:0].
4. SWD output regulator average current goes above the threshold set in register [Table 136, Register 0x1F](#) [7:0].
5. SWE output regulator average current goes above the threshold set in register [Table 182, Register 0x11A](#) [7:0].
6. SWF output regulator average current goes above the threshold set in register [Table 183, Register 0x11B](#) [7:0].

When either event occurs then PMIC sets the register [Table 114, Register 0x09](#) [3:0], [Table 175, Register 0x108](#) [5:4] appropriately, drives GSI_n output signal as shown in [Table 27](#) at the same time. The PMIC continues to operate as normal. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the GSI_n signal assertion. Once host determines the cause, the host may clear the appropriate output current consumption warning status register as well as any other status registers individually or by writing '1' to global status clear register in [Table 125, Register 0x14](#) [0] which triggers the GSI_n signal to be de-asserted. If the output current consumption warning condition is still present then PMIC will continue to assert GSI_n output signal and the appropriate status register in [Table 114, Register 0x09](#) [3:0], [Table 175, Register 0x108](#) [5:4] will remain at '1'. If the output current consumption warning condition persists, the host may set the appropriate mask register to remove GSI_n output signal as shown in [Table 28](#) and [Table 29](#).

6.21 PMIC LDO Output Failure

In the event where PMIC LDO outputs (VOUT_1.8V [Table 114, Register 0x09](#) [5] or VOUT_1.0V [Table 157, Register 0x33](#) [2]) failure occurs and PMIC cannot reliably support external communication, the PMIC has no control of CAMP signal and it is floated. The PMIC returns to "offline" state.

Note that the PMIC operation itself may not be guaranteed as PMIC internally may use the LDO output voltages for its own internal operation.

6.22 PMIC High Temperature Warning and Critical Temperature Protection

The PMIC provides a high temperature warning mechanism as well as critical temperature shutdown. There are two registers associated with PMIC temperature: The high temperature warning threshold register [Table 132, Register 0x1B](#) [2:0] and shutdown temperature threshold register [Table 151, Register 0x2E](#) [2:0]. The value programmed in the shutdown temperature register must be equal or greater than value programmed in a warning threshold register.

6.22 PMIC High Temperature Warning and Critical Temperature Protection (cont'd)

There is one possibility where PMIC recognizes the high temperature event.

1. The PMIC temperature goes above the threshold set in register [Table 132, Register 0x1B \[2:0\]](#).

When the above event occurs for a period longer than tHigh_Temp_Warning time, the PMIC sets the register [Table 114, Register 0x09 \[7\]](#) and drives GSI_n output signal as shown in [Table 27](#) at the same time. The PMIC continues to operate as normal. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the GSI_n signal assertion. Once host determines the cause, the host may clear the temperature warning status register as well as any other status registers individually or by writing '1' to global status clear register in [Table 125, Register 0x14 \[0\]](#) which triggers the GSI_n signal to be de-asserted. If the high temperature warning condition is still present then PMIC will continue to assert GSI_n output signal and the appropriate status register in [Table 114, Register 0x09 \[7\]](#) will remain at '1'. If the high temperature warning condition persists, the host may set the appropriate mask register to remove GSI_n output signal as shown in [Table 28](#) and [Table 29](#).

If the PMIC temperature goes above the threshold set in register [Table 151, Register 0x2E \[2:0\]](#) for a period longer than tShut_Down_Temp time, the PMIC internally generates VR Disable command and disables all of its switching output regulators as well as Vbias voltage regulator (optional), sets the code in register [Table 110, Register 0x05 \[2:0\]](#), updates [Table 113, Register 0x08 \[6\]](#), drives GSI_n and CAMP output signal as shown in [Table 27](#) at the same time. The PMIC keeps its VOUT_1.8V LDO and VOUT_1.0V LDO output regulator active. The host is responsible for taking any specific action. The host is expected to monitor the temperature status registers. When the temperature drops below the threshold, the host must re-start the PMIC by going through the power cycle of the VIN_Mgmt and VIN_Bulk input supply. If the PMIC is in VIN_Bulk input supply switchover state, the host must re-start the PMIC by going through the power cycle of the VIN_Bulk input supply.

6.23 VIN_Mgmt to VIN_Bulk Input Supply Switchover Event

After VR Enable command is registered, the PMIC automatically switches over from VIN_Mgmt to VIN_Bulk input supply under the following condition.

1. VIN_Mgmt goes below the threshold set in register [Table 152, Register 0x2F \[7\]](#).

When the above event occurs for a period longer than tInput_PWR_GOOD_GSI_Assertion time then PMIC sets the register [Table 114, Register 0x09 \[4\]](#) and drives GSI_n output signal as shown in [Table 27](#) at the same time. The PMIC continues to operate as normal. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the GSI_n signal assertion. Once host determines the cause, the host may clear the status register individually or by writing '1' to global status clear register in [Table 125, Register 0x14 \[0\]](#) which triggers the GSI_n signal to be de-asserted. No further action is needed by the host or the PMIC at this point.

Note that this event is treated differently by the PMIC. When host clears this event, the PMIC must remove the GSI_n signal assertion even though PMIC does not see valid VIN_Mgmt. This is to simplify host because host knows that there is no VIN_Mgmt and yet host expects the PMIC (as well as system) to continue to run normal and host should not have to worry about masking this event in PMIC. It is assumed that at some point VIN_Mgmt supply will come back up again, PMIC will detect it and assert GSI_n output signal as described in clause 6.24. At this point, PMIC will be ready to assert GSI_n output signal again if VIN_Mgmt input supply goes below the threshold set in register [Table 152, Register 0x2F \[7\]](#).

6.24 Valid VIN_Mgmt Supply Detection in Switchover Mode

When PMIC is in switchover mode as described in clause 6.23, the VIN_Mgmt input supply may power back up at any time. When VIN_Mgmt input supply re-powers back up, the PMIC sets the register [Table 157, Register 0x33](#) [4] and drives GSI_n output signal as shown in [Table 27](#) at the same time. The PMIC continues to operate as normal and automatically switches back to VIN_Mgmt input supply. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the GSI_n signal assertion. Once host determines the cause, the host may clear the status register individually or by writing '1' to global status clear register in [Table 125, Register 0x14](#) [0] which triggers the GSI_n signal to be de-asserted. No further action is needed by the host or the PMIC at this point.

Note that this event is treated differently by the PMIC. When host clears this event, the PMIC must remove the GSI_n signal assertion even though PMIC still sees valid VIN_Mgmt. This is to simplify host because host knows that VIN_Mgmt input supply is back and so host expects the PMIC (as well as system) to continue to run normal and host should not have to worry about masking this event in PMIC. It is assumed that if at some point VIN_Mgmt supply goes below the threshold again, PMIC will detect it and assert GSI_n output signal as described in Clause 6.23. At this point, PMIC will be ready to assert GSI_n output signal again if VIN_Mgmt input supply re-powers back up again.

6.25 Packet Error Code (PEC) and Parity Error Event

In I3C Basic mode, on PMIC's primary management interface, PEC function and Parity function can be enabled. If enabled, when PMIC detects either PEC error or Parity Error, the PMIC sets the register [Table 115, Register 0x0A](#) [3:2] appropriately, drives GSI_n output signal as shown in [Table 27](#) and it continues to operate as normal and allows access to all registers. See clauses 7.5.6 to 7.5.7 for additional details. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the GSI_n signal assertion. Once host determines the cause, the host may clear the status register individually or by writing '1' to global status clear register in [Table 125, Register 0x14](#) [0] which triggers the GSI_n signal to be de-asserted. No further action is needed by the host from this point on.

6.26 Analog to Digital Converter (ADC)

The PMIC supports analog to digital converter (ADC) to monitor input supply voltages (VIN_Bulk and VIN_Mgmt) as well as output voltage regulator voltage (SWA, SWB, SWC, SWD, SWE, SWF, VBIAS1 or VBIAS2, VOUT_1.8V and VOUT_1.0V). The register [Table 153, Register 0x30](#) [7:3] allows to enable the ADC and select the desired input supply voltage or output supply voltage. The register [Table 154, Register 0x31](#) [7:0] provides the actual voltage measurement. The accuracy of the voltage measurement is shown in [Table 30](#) and [Table 31](#).

Table 30 — PMIC Output ADC Voltage Accuracy

| Output Regulator: Voltage Range | SWA, SWB, SWC, SWE, SWF | SWD | 1.8V LDO 1.0V LDO | VBIAS1 or VBIAS2 |
|---------------------------------------|-------------------------|---------|----------------------|------------------|
| 1050mV to 1160mV | ± 1 LSB | N/A | N/A | N/A |
| Less than 1050mV; greater than 1160mV | ± 3 LSB | N/A | N/A | N/A |
| 1750mV to 1850mV | N/A | ± 1 LSB | N/A | N/A |
| Less than 1750mV; greater than 1850mV | N/A | ± 3 LSB | N/A | N/A |
| 1.8V LDO, 1.0V LDO | N/A | N/A | ± 3 LSB | N/A |
| VBIAS1 or VBIAS2 LDO | N/A | N/A | N/A | ± 6 LSB |

6.26 Analog to Digital Converter (ADC) (cont'd)

Table 31 — PMIC Input ADC Voltage Accuracy

| Input Voltage | |
|---------------|---------|
| VIN_Bulk | ± 6 LSB |
| VIN_Mgmt | ± 6 LSB |

The PMIC also monitors output voltage regulator current or power for SWA, SWB, SWC, SWD, SWE and SWF. The PMIC updates registers [Table 117, Register 0x0C \[7:0\]](#) to [Table 120, Register 0x0F \[7:0\]](#) for SWA to SWD respectively if [Table 155, Register 0x32 \[1:0\] = '00'](#) or register [Table 167, Register 0x100 \[7:0\]](#) to [Table 174, Register 0x107 \[7:0\]](#) for SWA to SWF respectively if [Table 155, Register 0x32 \[1:0\] = '01'](#).

The register [Table 132, Register 0x1B \[6\]](#) allows host to select whether PMIC should report current measurements or power measurements. The current or power measurement reported in this registers are an average measurement over vendor specific time period. If [Table 132, Register 0x1B \[6\] = '1'](#), the register [Table 131, Register 0x1A \[1\]](#) allows host to select whether PMIC should report individual rail power or total power in [Table 117, Register 0x0C \[7:0\]](#) if [Table 155, Register 0x32 \[1:0\] = '00'](#) or in [Table 168, Register 0x101 \[2:0\]](#) and [Table 169, Register 0x102 \[7:0\]](#) if [Table 155, Register 0x32 \[1:0\] = '01'](#).

The register update frequency of this register is configured in [Table 153, Register 0x30 \[1:0\]](#). The internal sampling rate of the PMIC is vendor specific.

The accuracy of the current or power measurement is shown in [Table 32](#) and [Table 33](#) depending on the setting of [Table 155, Register 0x32 \[1:0\]](#).

Table 32 — PMIC ADC Current and Power Accuracy; R32[1:0] = 00

| Load Current | SWA to SWD Rails - Current Accuracy ^[1] | SWA to SWD Rails - Corresponding Power Accuracy ^[1] | Total Power Accuracy |
|-------------------------------|--|--|----------------------|
| Less than 0.5A | ± 4 LSB | ± 7 LSB | ± 12 LSB |
| Greater than or equal to 0.5A | ± 3 LSB | ± 6 LSB | |

NOTE 1 These specs are per rail only.

Table 33 — PMIC ADC Current and Power Accuracy; R32[1:0] = 01

| Load Current | SWA to SWF Rails - Current Accuracy ^[1] | SWA to SWF Rails - Corresponding Power Accuracy ^[1] | Total Power Accuracy |
|-------------------------------|--|--|-------------------------|
| Less than 0.5A | ± 9 LSB | ± 15 LSB | ± 25 LSB ^[2] |
| Greater than or equal to 0.5A | ± 8 LSB | ± 12 LSB | |

NOTE 1 These specs are per rail only.

NOTE 2 This accuracy is guaranteed if the total power is less than or equal to 23 W. If the total power is greater than 23 W, the accuracy is ± 5% of total power.

6.27 PMIC Address ID (PID)

The PMIC has PID input pin which allows to assign up to three different unique ID for I²C and I³C Basic protocol.

At first power on, when VIN_Mgmt input is applied, the PMIC automatically senses its ID as shown in [Table 34](#).

Table 34 — PMIC ID

| PID Pin Connection on DIMM Board | PMIC ID | Comment |
|----------------------------------|------------|------------------------------------|
| short to GND | PID = 1001 | |
| Floating | PID = 1000 | |
| short to 1.8 | PID = 1100 | Connected to PMIC's VOUT_1.8V Rail |

6.28 Error Injection

The PMIC offers error injection function for the purpose of debug, test and validation at various stages.

Error Injection Function Usage prior to VR Enable:

- Prior to VR Enable command, the Error injection function may be invoked by setting error injection enable bit [Table 159, Register 0x35](#) [7] = '1' during the configuration state. If any of either VIN_Bulk UV/OV or SWx OV/UV or Critical Temp Shutdown or MTP (DIMM vendor or PMIC vendor) error is injected prior to VR Enable command, the PMIC shall not execute power on sequence and shall not enable PMIC output regulators when PMIC receives VR Enable command. The PMIC shall not update error log registers ([Table 108, Register 0x03](#) to [Table 112, Register 0x07](#)). The PMIC shall update appropriate status registers accordingly when error is injected.

Error Injection Function Usage after VR Enable:

- After PMIC output regulators are enabled with VR Enable command and PMIC is in non write-protect mode, the error injection function may be invoked by setting error injection enable bit [Table 159, Register 0x35](#) [7] = '1'. If any of either VIN_Bulk UV/OV or SWx OV/UV or Critical Temp Shutdown error is injected the PMIC shall execute Power Off Sequence to disable PMIC output regulators and shall update the error log registers ([Table 109, Register 0x04](#) [7:4] [Table 110, Register 0x05](#) to [Table 112, Register 0x07](#)) as well as status registers accordingly. Note that if any of the output rails are not enabled through power on sequence configuration registers, the error injection on that output rail does not apply. The PMIC shall not update [Table 108, Register 0x03](#) [7:0], [Table 109, Register 0x04](#) [3:0] and [Table 201, Register 0x140](#) [7:0] to [Table 230, Register 0x15D](#) [7:0]. The MTP (DIMM vendor or PMIC vendor error injection feature) is not allowed after VR Enable command.
- After PMIC output regulators are enabled with VR Enable command and PMIC is in write-protect mode, the error injection enabling [Table 159, Register 0x35](#) [7] = '1' is disallowed. The PMIC shall ignore any attempts to inject any error and shall not execute Power Off Sequence to disable PMIC output regulators and shall not update any error log or status registers.

To exit the error injection function, the host shall power cycle VIN_Bulk and VIN_Mgmt input supply.

6.29 Error Log Count Enhancement

The PMIC5030 enhances the global history of error log register definition by storing the detail fault information for first fifteen fault events. The history of fault information is not erasable by the controller. This enhances the PMIC's ability to debug the failure mechanism in the event when PMIC is returned to the PMIC vendor.

There is no change in the definition for [Table 109, Register 0x04 \[7:4\]](#) compared to previous generation of PMIC5020 or PMIC5000 or PMIC5010 definition.

The PMIC5030 defines the additional register [Table 109, Register 0x04 \[3:0\]](#) which indicates how many times the fault has occurred and for each fault it points to additional registers for detail log information as shown in the description for [Table 109, Register 0x04 \[3:0\]](#). When there are multiple buck regulator faults in one event (e.g., SWAB, SWE and SWF UV fault occurs at the same time) that causes the PMIC to turn off all the output regulators, it counts as one error and corresponding detail error log register captures all three faults.

When error injection function is applied, the PMIC updates [Table 109, Register 0x04 \[7:4\]](#), [Table 110, Register 0x05 \[7:0\]](#), [Table 111, Register 0x06 \[7:0\]](#), [Table 112, Register 0x07 \[7:0\]](#). The PMIC shall not update [Table 109, Register 0x04 \[3:0\]](#) and [Table 201, Register 0x140 \[7:0\]](#) to [Table 230, Register 0x15D \[7:0\]](#).

6.30 NVM MTP CRC Computation and Error Check

The PMIC has non-volatile MTP for DIMM vendor region and PMIC vendor specific region. The PMIC5030 shall perform the non-volatile MTP memory error check at first power on when VIN_Mgmt input supply is applied. The PMIC checks for MTP memory error (due to memory loss or bit flipping or any other internal functional or timing fault related to MTP memory) to ensure that PMIC does not inadvertently turn on the regulators with incorrect MTP memory content. This increases the PMIC reliability in the system.

The PMIC performs two independent checks. One for DIMM vendor memory region and other for PMIC vendor memory region.

6.30.1 DIMM Vendor Region MTP Check

During the assembly phase of the DIMM, the DIMM vendor programs the entire DIMM region; computes and programs the 8-bit CRC code in [Table 277, Register 0x6F \[7:0\]](#) using the polynomial as noted below. The seed value is all zero.

$$C(X) = X^8 + X^2 + X^1 + 1$$

The CRC computation shall include the DIMM vendor region as shown below in the exact same order. All reserved bits must be included as '0' in the computation. Total of 376 bits.

- R40 [7:0], R41 [7:0], R42 [7:0], ..., R4E [7:0], R4F [7:0]
- R50 [7:0], R51 [7:0], R52 [7:0], ..., R5E [7:0], R5F [7:0]
- R60 [7:0], R61 [7:0], R62 [7:0], ..., R6E [7:0]

The PMIC performs DIMM vendor region MTP memory check at power on and sets the [Table 177, Register 0x10A \[7\]](#) = '1' to inform controller that PMIC has performed this check. The PMIC performs the same computation of the DIMM vendor region as noted above to generate the 8-bit CRC code and compares it against what the DIMM vendor has programmed in [Table 277, Register 0x6F \[7:0\]](#).

If there is no mismatch in CRC code, the PMIC keeps [Table 177, Register 0x10A \[6\]](#) = '0' and allows normal operation to enable the output regulators.

6.30.1 DIMM Vendor Region MTP Check (cont'd)

If there is mismatch in CRC code, the PMIC sets the [Table 177, Register 0x10A \[6\]](#) = '1' and blocks PMIC to turn on the regulator with any method (via I²C/I³C bus command or via VR_OE pin or Auto turn on) if [Table 163, Register 0x3A \[1\]](#) = '0'. The PMIC also updates the error counter in [Table 108, Register 0x03 \[7:4\]](#). All VR Enable commands from this point on are ignored by the PMIC. At this point, there are three options controller may take:

- Re-cycle the power to the PMIC and try again.
- Isolate and map out the PMIC as described in Section 10.
- Instruct PMIC to bypass the DIMM CRC Error Status in [Table 177, Register 0x10A \[6\]](#) by setting [Table 163, Register 0x3A \[1\]](#) = '1' and execute subsequent VR Enable command to turn on the regulators.

The status registers [Table 177, Register 0x10A \[7:6\]](#) cannot be cleared by the controller. The error log register [Table 108, Register 0x03 \[7:4\]](#) cannot be cleared by the controller and MTP cannot be erased by the controller.

Note that only if the status register [Table 177, Register 0x10A \[6\]](#) = '1', the PMIC blocks the VR enable command. The error log register [Table 108, Register 0x03 \[7:4\]](#) does not block the VR enable command.

When error injection function is applied, the PMIC shall not update [Table 108, Register 0x03 \[7:4\]](#); it only updates [Table 177, Register 0x10A \[6\]](#) = '1'. This error injection feature is only allowed prior to VR Enable command.

6.30.2 PMIC Vendor Region MTP Check

The PMIC vendor region memory check is implementation specific. The PMIC may choose to implement similar method as DIMM vendor region where it may compute and program the 8-bit CRC code in its own proprietary register space and check at power on. Alternatively, PMIC may choose to implement a different method.

Regardless of which method PMIC chooses to implement, the PMIC shall check and guarantee that its memory content is valid at power on. If there is an error in PMIC's own memory content, PMIC sets [Table 177, Register 0x10A \[4\]](#) = '1' and blocks PMIC to turn on the regulator with any method (via I²C/I³C bus command or via VR_OE pin or Auto turn on). The PMIC also updates the error counter in [Table 108, Register 0x03 \[3:0\]](#). All VR Enable command from this point on are ignored by the PMIC. At this point, the controller may take one of the two options as noted in Clause 6.30.1.

The status registers [Table 177, Register 0x10A \[5:4\]](#) cannot be cleared by the controller. The error log register [Table 108, Register 0x03 \[3:0\]](#) cannot be cleared by the controller and MTP cannot be erased by the controller.

Note that only if the status register [Table 177, Register 0x10A \[4\]](#) = '1', the PMIC blocks the VR enable command. The error log register [Table 108, Register 0x03 \[3:0\]](#) does not block the VR enable command.

When error injection function is applied, the PMIC shall not update [Table 108, Register 0x03 \[3:0\]](#); it only updates [Table 177, Register 0x10A \[4\]](#) = '1'. This error injection feature is only allowed prior to VR Enable command.

6.30.3 DIMM Vendor Region CRC Check on Demand

During the assembly phase of the DIMM, the DIMM vendor programs the entire DIMM region including the 8-bit CRC code as described in Clause 6.30.1. To aid DIMM vendor to make sure that DIMM vendor region value and the corresponding CRC code is correct prior to burning the DIMM vendor region and the 8-bit CRC code, the PMIC offers a mechanism to do a test to ensure there is no error in CRC code. The steps are outlined as follows:

6.30.3 DIMM Vendor Region CRC Check on Demand (cont'd)

1. DIMM vendor computes 8-bit CRC code of the DIMM region (0x40 to 0x6E)
2. DIMM vendor writes entire DIMM region including the CRC code (R0x40 to R0x6F) in the PMIC. At this point, the burn command is not issued.
3. Write [Table 163, Register 0x3A](#) [0] = '1' to instruct PMIC to compute 8-bit CRC code of DIMM region (0x40 to 0x6E) and check against the value programmed in R0x6F.
4. PMIC sets [Table 176, Register 0x109](#) [0] = '1' if 8-bit CRC code it computed does not match with the 8-bit CRC code written by the DIMM vendor in [Table 277, Register 0x6F](#); if there is a match, the PMIC keeps the [Table 176, Register 0x109](#) [0] = '0'.
5. DIMM vendor reads the [Table 176, Register 0x109](#) [0] status. If it is set to '1', the DIMM vendor clears this status register by writing [Table 179, Register 0x10F](#) [0] = '1' and repeats steps 1 to 3. If it is '0', the DIMM vendor performs the burn command by writing [Table 162, Register 0x39](#) for each of the three blocks.

7 I²C and I3C Basic Interface Operation

At power on, by default, the PMIC device comes up in legacy I²C mode of operation. Following applies in I²C mode:

1. The maximum operation speed is limited to 1 MHz
2. In-band interrupts are not supported
3. Bus reset is supported.
4. Parity check is not supported except for supported CCCs.
5. Packet Error check is not supported.

The PMIC device shall operate in the legacy I²C mode until put into I3C Basic mode via command.

The host may put the PMIC device in I3C Basic mode by issuing SETAASA CCC.

Following applies in I3C Basic mode.

1. The max operation speed is up to 12.5 MHz
2. In-band interrupts are supported
3. Bus reset is supported.
4. Parity check is always enabled by default.
5. Packet error check is supported and by default is disabled.

7.1 Device Interface - Protocol

The 7-bit serial address of the PMIC device applies to both I²C and I3C Basic mode of operation identically.

7.1.1 PMIC Management Bus

The PMIC supports two different protocols on its management bus.

- I²C Target Protocol - Speed Up to 1 MHz
- I3C Basic Target Protocol - Speed Up to 12.5 MHz

The PMIC's 7-bit target address [7:1] is composed of 4-bit LID address [7:4] and 3-bit HID address [3:1].

Table 35 — 7-bit Address of PMIC Device

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------------------|-------|-------|-------|---------------|-------|-------|------------|
| 1 | x | 0 | x | 1 | 1 | 1 | R/W |
| PMIC Device Type ID (LID) | | | | Host ID (HID) | | | Read/Write |

7.1.1 PMIC Management Bus (cont'd)

The PMIC's 4-bit [7:4] LID address is:

- If PID pin is connected to GND on PCB: '1001'
- If PID pin is tied to 1.8 V on PCB: '1100'
- If PID pin is floating on PCB: '1000'

The PMIC's 3-bit [3:1] HID address is per [Table 158, Register 0x34 \[3:1\]](#).

The PMIC device samples the status of the PID pin on power up. The sampled status of the PID pin is used to select one of the three possible unique LID code for the device. The selected LID code either '1001' or '1100' or '1000' is merged with a 3 bit HID code from [Table 158, Register 0x34 \[3:1\]](#) to establish the 7-bit address code the device. For example, with the default setting in [Table 158, Register 0x34 \[3:1\]](#) = '111'; if the PID pin is connected to GND, the device address shall be '1001 111'.

7.1.2 Switch from I²C Mode to I3C Basic Mode

By default when PMIC first powers on, it operates in legacy I²C mode. The PMIC device shall operate in I²C mode until put into I3C Basic mode via command.

In I²C mode, the host is allowed to issue only 3 CCCs (DEVCTRL, SETHID, SETAASA). All other CCCs are not supported and the PMIC device may simply ignore it. The Host must issue DEVCTRL and SETHID CCC first (if required) followed by SETAASA CCC.

The Host puts the PMIC device in I3C Basic mode by issuing SETAASA CCC.

When SETAASA CCC is registered by the PMIC device, it updates the [Table 155, Register 0x32 \[6\]](#) to '1'.

When SETHID CCC is registered by the PMIC device, it updates the [Table 158, Register 0x34 \[3:1\]](#).

7.1.3 Switch from I3C Basic Mode to I²C Mode

The Host can put the PMIC device back in I²C mode from I3C Basic mode at any time by issuing RSTDAA CCC.

When RSTDAA CCC is registered by the PMIC device, it updates the [Table 155, Register 0x32 \[6\]](#) to '0'.

7.2 Configuration Register Addressing

At first power on, by default, the PMIC accepts one byte address which covers first 256 bytes of configuration registers. To address configuration registers beyond first 256 bytes (up to 4096 bytes), the PMIC must be in a two byte address mode. The two byte address mode is configured by setting [Table 153, Register 0x30 \[2\]](#) = '1'. The PMIC supports one byte and two byte address mode in both I2C and I3C mode of operation.

The PMIC returns to one byte address mode when Bus Reset event occurs or when it registers RSTDAA CCC.

7.3 I²C Target Protocol

The PMIC device operates on a standard I²C serial interface. Transactions where the PMIC device is the targeted target device begin with the Host issuing a START condition followed by a 7-bit PMIC device address then a read or write bit, RW. All data are transmitted with the most significant bit MSB first. During the address followed by R/W bit transmission, the PMIC device typically replies with an ACK unless there are exceptional conditions when it may passively assert a NACK.

The PMIC device host region registers that are write-protected in write-protect mode of operation, the PMIC ACKs the host request but the PMIC does not execute the operation internally.

Similarly, regardless of write-protect mode or non write-protect mode of operation, without the correct password, all DIMM vendor and vendor specific region registers are write-protected and PMIC ACKs the host request but the PMIC does not execute the operation internally.

The PMIC device accepts 1 byte of address which covers 256 bytes of registers. The PMIC device register space does not require page selection process as all registers are within first 256 bytes.

7.3.1 Write Operation - Data Packet

The PMIC supports Byte Write or Block Write operation as shown in [Table 36](#) and [Table 37](#) for one byte and two byte address mode respectively. For Byte Write operation, only one data byte is transferred followed by Stop operation.

Table 36 — Write Command Data Packet; 1 Byte Address Mode

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N | Stop |
|------------------------|---------------|-------|-------|-------|-------|-------|-------|-------|-----|------|
| S or Sr ^[1] | 1 | X | 0 | X | HID | | | W=0 | A | |
| | Address [7:0] | | | | | | | | A | |
| | Data | | | | | | | | A | |
| | ... | | | | | | | | A | |
| | Data | | | | | | | | A | |

NOTE 1 In I²C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I²C mode. Any other operation including another Repeat Start is considered an illegal operation; the PMIC may ignore it and still ACK or it may NACK.

Table 37 — Write Command Data Packet; 2 Byte Address Mode

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|------------------------|---------------|-------|-------|-------|----------------|-------|-------|-------|-------|------|
| S or Sr ^[1] | 1 | X | 0 | X | HID | | | W=0 | A | |
| | Address [7:0] | | | | | | | | A | |
| | 0 | 0 | 0 | 0 | Address [11:8] | | | A | | |
| | Data | | | | | | | | A | |
| | Data | | | | | | | | A | |
| | ... | | | | | | | | A | |
| | Data | | | | | | | | A | |

NOTE 1 In I²C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I²C mode. Any other operation including another Repeat Start is considered an illegal operation; the PMIC may ignore it and still ACK or it may NACK.

7.3.2 Read Operation - Data Packet

The PMIC supports Byte Read or Block Read operation as shown in Table 38 and Table 39 for one byte and two address mode respectively. For Byte Read operation, only one data byte is transferred followed by Stop operation.

Table 38 — Read Command Data Packet; 1 Byte Address Mode

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N | Stop |
|------------------------|---------------|-------|-------|-------|-------|-------|-------|-------|------------------|------|
| S or Sr ^[1] | 1 | X | 0 | X | HID | | | W=0 | A | |
| | Address [7:0] | | | | | | | | A | |
| Sr | 1 | X | 0 | X | HID | | | R=1 | A ^[2] | |
| | Data | | | | | | | | A | |
| | ... | | | | | | | | A | |
| | Data | | | | | | | | N ^[3] | P |

NOTE 1 In I²C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I²C mode. Any other operation including another Repeat Start is considered an illegal operation; the PMIC may ignore it and still ACK or it may NACK.

NOTE 2 If target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. The PMIC may eventually ACK.

NOTE 3 When PMIC device reaches last byte within the region (either Host region or DIMM vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for DIMM vendor region or Vendor specific region. Once the address counter reaches 0x1FF, it will reset to address 0x00 and it will continue to return the data. Only Host can perform STOP operation.

Table 39 — Read Command Data Packet; 2 Byte Address Mode

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N | Stop |
|------------------------|---------------|-------|-------|-------|----------------|-------|-------|-------|------------------|---------|
| S or Sr ^[1] | 1 | X | 0 | X | HID | | | W=0 | A | |
| | Address [7:0] | | | | | | | | A | |
| | 0 | 0 | 0 | 0 | Address [11:8] | | | A | | |
| Sr | 1 | X | 0 | X | HID | | | R=1 | A ^[2] | |
| | Data | | | | | | | | A | |
| | Data | | | | | | | | A | |
| | ... | | | | | | | | A | |
| | Data | | | | | | | | N ^[3] | Sr or P |

NOTE 1 In I²C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I²C mode. Any other operation including another Repeat Start is considered an illegal operation; the PMIC may ignore it and still ACK or it may NACK.

NOTE 2 If the PMIC NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. The PMIC may eventually ACK.

NOTE 3 When PMIC device reaches last byte within the region (either Host region or DIMM vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for DIMM vendor region or Vendor specific region. Once the address counter reaches 0x1FF, it will reset to address 0x00 and it will continue to return the data. Only Host can perform STOP operation.

7.3.3 Default Read Address Pointer Mode

During normal operation of the DDR5 DIMM, the host periodically may poll critical information from the same location. An example may be the PMIC device's status registers or current or power measurement register readout. To help improve the efficiency of the I²C bus protocol, the PMIC offers a default read address pointer mode so that whenever the PMIC device sees the STOP operation on its SCL and SDA bus, its read address pointer is always resets to default address. The default read pointer address mode is enabled through register [Table 163, Register 0x3A](#) [6] and default starting address for read operation is selectable through register [Table 163, Register 0x3A](#) [5:4]. This allows host to read the read command data packet as shown in [Table 40](#). The default read address pointer reduces the packet overhead by 2 bytes. The host typically enables this mode at last after VR Enable command when the normal operation of the DDR5 DIMM begins.

Table 40 — Read Command Data Packet with Default Address Pointer Mode

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N | Stop |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|------------------|------|
| S or Sr | 1 | X | 0 | X | HID | | | R=1 | A | |
| | Data | | | | | | | | A | |
| | ... | | | | | | | | A | |
| | Data | | | | | | | | N ^[1] | P |

NOTE 1 When PMIC device reaches last byte within the region (either Host region or DIMM vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for DIMM vendor region or Vendor specific region. Once the address counter reaches 0x1FF, it will reset to address 0x00 and it will continue to return the data. Only Host can perform STOP operation.

7.4 I3C Basic Target Protocol

7.4.1 Write Operation Data Packet

The PMIC device operates on a standard I3C Basic serial interface. Transactions where the PMIC device is the targeted target device begin with the Host issuing a START condition followed by a 7-bit PMIC device address then a read or write bit, RW. All data are transmitted with the most significant bit MSB first. During the address followed by R/W bit transmission, the PMIC device typically replies with an ACK unless there are exceptional conditions when it may passively assert a NACK. See [Table 41](#). The "T" bit carries Parity information from the Host for each byte.

The PMIC device host region registers that are write-protected in write-protect mode of operation, the PMIC does not execute the operation internally.

Similarly, regardless of write-protect mode or non- write-protect mode of operation, without the correct password, all DIMM vendor and vendor specific region registers are write-protected and PMIC does not execute the operation internally.

The Packet Error Code (PEC) function is disabled by default when the PMIC device is put in I3C Basic mode. The host may optionally enable this function through [Table 158, Register 0x34](#) [7] or DEVCTRL CCC. If enabled, the PEC is appended at the end of all transactions. If PEC is enabled, the host must complete the burst length as indicated in CMD field. In other words, the host must not interrupt the burst length prematurely for Write operation.

7.4.1 Write Operation Data Packet (cont'd)

Table 41 — Write Command Data Packet; PEC Disabled; 1 Byte Address Mode

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|---------------|-------|-------|-------|-------|-------|-------|-------|--------------------------|------|
| S or Sr | 1 | X | 0 | X | HID | | | W=0 | A ^{[1],[2],[3]} | |
| | Address [7:0] | | | | | | | | T | |
| | Data | | | | | | | | T | |
| | ... | | | | | | | | T | |
| | Data | | | | | | | | T | |

- NOTE 1 See [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Address bit 7).
- NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
- NOTE 3 The PMIC device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.
- NOTE 4 Repeat Start or Repeat Start with 7'h7E.

Table 42 — Write Command Data Packet; PEC Disabled; 2 Byte Address Mode

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|---------------|-------|-------|-------|----------------|-------|-------|-------|--------------------------|------------------------|
| S or Sr | 1 | X | 0 | X | HID | | | W=0 | A ^{[1].[2].[3]} | |
| | Address [7:0] | | | | | | | | T | |
| | 0 | 0 | 0 | 0 | Address [11:8] | | | T | | |
| | Data | | | | | | | | T | |
| | ... | | | | | | | | T | |
| | Data | | | | | | | | T | Sr ^[4] or P |

- NOTE 1 See [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).
- NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
- NOTE 3 The PMIC device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.
- NOTE 4 Repeat Start or Repeat Start with 7'h7E.

7.4.1 Write Operation Data Packet (cont'd)

Table 43 — Write Command Data Packet; PEC Enabled; 1 Byte Address Mode

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|---------------|-------|-------|-------|-------|-------|-------|-------|--------------------------|------------------------|
| S or Sr | 1 | X | 0 | X | HID | | | W=0 | A ^{[1],[2],[3]} | |
| | Address [7:0] | | | | | | | | T | |
| | CMD | | | W=0 | 0000 | | | T | | |
| | Data | | | | | | | | T | |
| | ... | | | | | | | | T | |
| | Data | | | | | | | | T | |
| | PEC | | | | | | | | T | Sr ^[4] or P |

NOTE 1 See [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Address bit 7).

NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 Repeat Start or Repeat Start with 7'h7E.

Table 44 — Write Command Data Packet; PEC Enabled; 2 Byte Address Mode

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|---------------|-------|-------|-------|----------------|-------|-------|-------|--------------------------|------------------------|
| S or Sr | 1 | X | 0 | X | HID | | | W=0 | A ^{[1],[2],[3]} | |
| | Address [7:0] | | | | | | | | T | |
| | CMD | | | W=0 | Address [11:8] | | | T | | |
| | Data | | | | | | | | T | |
| | ... | | | | | | | | T | |
| | Data | | | | | | | | T | |
| | PEC | | | | | | | | T | Sr ^[4] or P |

NOTE 1 See [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 Repeat Start or Repeat Start with 7'h7E.

The host may optionally allow PMIC device to request IBI. For this case, the transactions to the PMIC device begin with the I3C host issuing a START condition followed by 7'h7E and then write bit. If PMIC device has a pending IBI, it transmits its 7-bit device select code followed by R=1. If PMIC device has no pending IBI, there is no action taken by PMIC. [Table 45](#) and [Table 47](#) show the I3C Basic bus write command data packet with optional IBI header for PEC disabled and PEC enabled case respectively. Note that in [Table 47](#), PEC calculation does not include IBI header byte (7'h7E followed by W=0).

7.4.1 Write Operation Data Packet (cont'd)

**Table 45 — Write Command Data Packet with IBI Header; No Pending IBI, PEC Disabled;
1 Byte Address Mode**

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|-------|---------------|-------|-------|-------|-------|-------|-------|-------|------------------------|------------------------|
| S | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^{[1],[2]} | |
| Sr | 1 | X | 0 | X | HID | | | W=0 | A ^{2,[3],[4]} | |
| | Address [7:0] | | | | | | | | T | |
| | Data | | | | | | | | T | |
| | ... | | | | | | | | T | |
| | Data | | | | | | | | T | Sr ^[5] or P |

- NOTE 1 See [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start)
- NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
- NOTE 3 See [Figure 24](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and See [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Address bit 7).
- NOTE 4 The PMIC device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.
- NOTE 5 Repeat Start or Repeat Start with 7'h7E.

**Table 46 — Write Command Data Packet with IBI Header; No Pending IBI, PEC Disabled;
2 Byte Address Mode**

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|-------|---------------|-------|-------|-------|----------------|-------|-------|-------|------------------------|------------------------|
| S | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^{[1],[2]} | |
| Sr | 1 | X | 0 | X | HID | | | W=0 | A ^{2,[3],[4]} | |
| | Address [7:0] | | | | | | | | T | |
| | 0 | 0 | 0 | 0 | Address [11:8] | | | T | | |
| | Data | | | | | | | | T | |
| | ... | | | | | | | | T | |
| | Data | | | | | | | | T | Sr ^[5] or P |

- NOTE 1 See [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Repeat Start).
- NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
- NOTE 3 See [Figure 24](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).
- NOTE 4 The PMIC device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.
- NOTE 5 Repeat Start or Repeat Start with 7'h7E.

7.4.1 Write Operation Data Packet (cont'd)

Table 47 — Write Command Data Packet with IBI Header; No Pending IBI, PEC Enabled; 1 Byte Address Mode

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|-------|---------------|-------|-------|-------|-------|-------|-------|-------|------------------------|------------------------|
| S | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^{[1],[2]} | |
| Sr | 1 | X | 0 | X | HID | | | W=0 | A ^{2,[3],[4]} | |
| | Address [7:0] | | | | | | | | T | |
| | CMD | | | W=0 | 0000 | | | | T | |
| | Data | | | | | | | | T | |
| | ... | | | | | | | | T | |
| | Data | | | | | | | | T | |
| | PEC | | | | | | | | T | Sr ^[5] or P |

- NOTE 1 See [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start)
- NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
- NOTE 3 See [Figure 24](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and See [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Address bit 7).
- NOTE 4 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.
- NOTE 5 Repeat Start or Repeat Start with 7'h7E.

Table 48 — Write Command Data Packet with IBI Header; No Pending IBI, PEC Enabled; 2 Byte Address Mode

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|-------|---------------|-------|-------|-------|----------------|-------|-------|-------|------------------------|------|
| S | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^{[1],[2]} | |
| Sr | 1 | X | 0 | X | HID | | | W=0 | A ^{2,[3],[4]} | |
| | Address [7:0] | | | | | | | | T | |
| | CMD | | | W=0 | Address [11:8] | | | | T | |
| | Data | | | | | | | | T | |
| | ... | | | | | | | | T | |
| | Data | | | | | | | | T | |
| | PEC | | | | | | | | T | |

- NOTE 1 See [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Repeat Start).
- NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
- NOTE 3 See [Figure 24](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).
- NOTE 4 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.
- NOTE 5 Repeat Start or Repeat Start with 7'h7E.

7.4.2 Read Operation - Data Packet

The PMIC device operates on a standard I3C Basic serial interface. Transactions where the PMIC device is the targeted target device begin with the Host issuing a START condition followed by a 7-bit PMIC device address then a read or write bit, RW. All data are transmitted with the most significant bit MSB first. During the address followed by R/W bit transmission, the PMIC device typically replies with an ACK unless there are exceptional conditions when it may passively assert a NACK. See Table 49. The “T” bit carries Parity information from the Host for each byte prior to Repeat START. After Repeat START, “T” bit carries information from PMIC device to Host indicating Continuous (‘1’) or Stop (‘0’) whether it is transmitting the last byte or not.

The Packet Error Code (PEC) function is disabled by default when the PMIC device is put in I3C Basic mode. The host may optionally enable this function through Table 158, Register 0x34 [7] or DEVCTRL CCC. If enabled, the PEC is appended as shown in Table 49. If PEC is enabled, the host must complete the burst length as indicated in CMD field. In other words, the host must not interrupt the burst length prematurely for Read operation.

Table 49 — Read Command Data Packet; PEC Disabled; 1 Byte Address Mode

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|---------------|-------|-------|-------|-------|-------|-------|-------|--------------------------|------------------------|
| S or Sr | 1 | X | 0 | X | HID | | | W=0 | A ^{[1],[2],[3]} | |
| | Address [7:0] | | | | | | | | T | |
| Sr | 1 | X | 0 | X | HID | | | R=1 | A/N ^{[4],[5]} | |
| | Data | | | | | | | | T=1 | |
| | ... | | | | | | | | T=1 | |
| | Data | | | | | | | | T=1 ^{[6],[7]} | Sr ^[8] or P |

- NOTE 1 See Figure 22 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Address bit 7).
- NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
- NOTE 3 The PMIC device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.
- NOTE 4 If target device NACKs during Repeat Start for any reason, the host may retry Repeat Start again. The host can do the Repeat Start as many times it may desire. If target device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity errors, the PMIC may eventually ACK.
- NOTE 5 See Figure 24 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
- NOTE 6 See Figure 25 to see how Host ends target device operation.
- NOTE 7 When PMIC device reaches last byte within the region (either Host region or DIMM vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for DIMM vendor region or Vendor specific region. Once the address counter reaches 0x1FF, it will reset to address 0x00 and it will continue to return the data. Only Host can perform STOP operation.
- NOTE 8 Repeat Start or Repeat Start with 7'h7E.

7.4.2 Read Operation - Data Packet (cont'd)

Table 50 — Read Command Data Packet; PEC Disabled; 2 Byte Address Mode

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|---------------|-------|-------|-------|----------------|-------|-------|-------|--------------------------|------------------------|
| S or Sr | 1 | X | 0 | X | HID | | | W=0 | A ^{[1],[2],[3]} | |
| | Address [7:0] | | | | | | | | T | |
| | 0 | 0 | 0 | 0 | Address [11:8] | | | T | | |
| Sr | 1 | X | 0 | X | HID | | | R=1 | A/N ^{[4],[5]} | |
| | Data | | | | | | | | T=1 | |
| | ... | | | | | | | | T=1 | |
| | Data | | | | | | | | T=1 ^{[6],[7]} | Sr ^[8] or P |

NOTE 1 See [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 If PMIC device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If PMIC device NACKs due to parity error, it will always NACK regardless of how many times the host tries Repeat Start. If there were no parity errors, the device may eventually ACK.

NOTE 5 See [Figure 24](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 6 See [Figure 25](#) to see how Host ends target device operation.

NOTE 7 When PMIC device reaches last byte within the region (either Host region or DIMM Vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for DIMM Vendor region or Vendor Specific region. Once the address counter reaches 0x1FF, it will reset to address 0x00 and it will continue to return the data. Only host can perform the STOP operation.

NOTE 8 Repeat Start or Repeat Start with 7'h7E.

7.4.2 Read Operation - Data Packet (cont'd)

Table 51 — Read Command Data Packet; PEC Enabled; 1 Byte Address Mode

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|---------------|-------|-------|-------|-------|-------|-------|-------|--------------------------|------------------------|
| S or Sr | 1 | X | 0 | X | HID | | | W=0 | A ^{[1],[2],[3]} | |
| | Address [7:0] | | | | | | | | T | |
| | CMD | | | R=1 | 0000 | | | T | | |
| | PEC | | | | | | | | T | |
| Sr | 1 | X | 0 | X | HID | | | R=1 | A/N ^{[4],[5]} | |
| | Data | | | | | | | | T=1 | |
| | ... | | | | | | | | T=1 | |
| | Data | | | | | | | | T=1 | |
| | PEC | | | | | | | | T=0 ^[6] | Sr ^[7] or P |

NOTE 1 See [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Address bit 7).

NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 If target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If target device NACKs due to PEC error or parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the PMIC may eventually ACK. The PEC calculation by the target device only includes device select code of the ACK response of the Repeat start operation. In other words, if there are more than one Repeat Start operation, the target device includes device select of only the last Repeat Start from the Host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.

NOTE 5 See [Figure 24](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 6 See [Figure 26](#) to see how target device ends the operation followed by Host STOP operation.

NOTE 7 Repeat Start or Repeat Start with 7'h7E.

7.4.2 Read Operation - Data Packet (cont'd)

Table 52 — Read Command Data Packet; PEC Enabled; 2 Byte Address Mode

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|---------------|-------|-------|-------|----------------|-------|-------|-------|--------------------------|------------------------|
| S or Sr | 1 | X | 0 | X | HID | | | W=0 | A ^{[1],[2],[3]} | |
| | Address [7:0] | | | | | | | | T | |
| | CMD | | | R=1 | Address [11:8] | | | T | | |
| | PEC | | | | | | | | T | |
| Sr | 1 | X | 0 | X | HID | | | R=1 | A/N ^{[4],[5]} | |
| | Data | | | | | | | | T=1 | |
| | ... | | | | | | | | T=1 | |
| | Data | | | | | | | | T=1 | |
| | PEC | | | | | | | | T=0 ^[6] | Sr ^[7] or P |

NOTE 1 See [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 If PMIC device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If PMIC device NACKs due to PEC error or parity error, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the device may eventually ACK. The PEC calculation by the PMIC device only includes device select code of the ACK response of the Repeat Start operation. In other words, if there are more than one Repeat Start operation, the PMIC device includes device select of only the last Repeat Start from the host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.

NOTE 5 See [Figure 24](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 6 See [Figure 26](#) to see how Host ends target device operation followed by Host STOP operation.

NOTE 7 Repeat Start or Repeat Start with 7'h7E.

The host may optionally allow PMIC device to request IBI. For this case, the transactions to the PMIC device begin with the I3C Basic host issuing a START condition followed by 7'h7E and then write bit. If PMIC device has a pending IBI, it transmits its 7-bit device select code followed by R=1. If PMIC device has no pending IBI, there is no action taken by PMIC. [Table 53](#) and [Table 55](#) show the I3C Basic bus read command data packet with optional IBI header for PEC disabled and PEC enabled case respectively. Note that in [Table 55](#), PEC calculation does not include IBI header byte (7'h7E followed by W=0).

7.4.2 Read Operation - Data Packet (cont'd)

**Table 53 — Read Command Data Packet with IBI Header; No Pending IBI, PEC Disabled;
1 Byte Address Mode**

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|-------|---------------|-------|-------|-------|-------|-------|-------|-------|------------------------|------------------------|
| S | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^{[1],[2]} | |
| Sr | 1 | X | 0 | X | HID | | | W=0 | A ^{2,[3],[4]} | |
| | Address [7:0] | | | | | | | | T | |
| Sr | 1 | X | 0 | X | HID | | | R=1 | A/N ^{[5],[6]} | |
| | Data | | | | | | | | T=1 | |
| | ... | | | | | | | | T=1 | |
| | Data | | | | | | | | T=1 ^{[7],[8]} | Sr ^[9] or P |

- NOTE 1 See [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
- NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
- NOTE 3 See [Figure 24](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and See [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Address bit 7).
- NOTE 4 The PMIC device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.
- NOTE 5 See [Figure 24](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
- NOTE 6 If target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If target device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start.
- NOTE 7 See [Figure 25](#) to see how Host ends target device operation.
- NOTE 8 When PMIC device reaches last byte within the region (either Host region or DIMM vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for DIMM vendor region or Vendor specific region. Once the address counter reaches 0x1FF, it will reset to address 0x00 and it will continue to return the data. Only Host can perform STOP operation.
- NOTE 9 Repeat Start or Repeat Start with 7'h7E.

7.4.2 Read Operation - Data Packet (cont'd)

**Table 54 — Read Command Data Packet with IBI Header; No Pending IBI; PEC Disabled;
2 Byte Address Mode**

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|-------|---------------|-------|-------|-------|----------------|-------|-------|-------|------------------------|------------------------|
| S | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^{[1],[2]} | |
| Sr | 1 | X | 0 | X | HID | | | W=0 | A ^{2,[3],[4]} | |
| | Address [7:0] | | | | | | | | T | |
| | 0 | 0 | 0 | 0 | Address [11:8] | | | T | | |
| Sr | 1 | X | 0 | X | HID | | | R=1 | A/N ^{[5],[6]} | |
| | Data | | | | | | | | T=1 | |
| | ... | | | | | | | | T=1 | |
| | Data | | | | | | | | T=1 ^{[7],[8]} | |
| | | | | | | | | | | Sr ^[9] or P |

- NOTE 1 See [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Repeat Start).
- NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
- NOTE 3 See [Figure 24](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).
- NOTE 4 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.
- NOTE 5 See [Figure 24](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
- NOTE 6 If PMIC device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If PMIC device NACKs due to parity error, it will always NACK regardless of how many times the host tries Repeat Start. If there were no parity errors, the device may eventually ACK.
- NOTE 7 See [Figure 25](#) to see how Host ends target device operation.
- NOTE 8 When PMIC device reaches last byte within the region (either Host region or DIMM Vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for DIMM Vendor region or Vendor Specific region. Once the address counter reaches 0x1FF, it will reset to address 0x00 and it will continue to return the data. Only host can perform the STOP operation.
- NOTE 9 Repeat Start or Repeat Start with 7'h7E.

7.4.2 Read Operation - Data Packet (cont'd)

**Table 55 — Read Command Data Packet with IBI Header; No Pending IBI, PEC Enabled;
1 Byte Address Mode**

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|-------|---------------|-------|-------|-------|-------|-------|-------|-------|------------------------|------|
| S | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^{[1],[2]} | |
| Sr | 1 | X | 0 | X | HID | | | W=0 | A2 ^{[3],[4]} | |
| | Address [7:0] | | | | | | | | T | |
| | CMD | | | R=1 | 0000 | | | T | | |
| | PEC | | | | | | | | T | |
| Sr | 1 | X | 0 | X | HID | | | R=1 | A/N ^{[5],[6]} | |
| | Data | | | | | | | | T=1 | |
| | ... | | | | | | | | T=1 | |
| | Data | | | | | | | | T=1 | |
| | PEC | | | | | | | | T=0 ^[7] | |

- NOTE 1 See [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
- NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
- NOTE 3 See [Figure 24](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and See [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Address bit 7).
- NOTE 4 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.
- NOTE 5 See [Figure 24](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
- NOTE 6 If target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If target device NACKs due to PEC error or parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the PMIC may eventually ACK. The PEC calculation by the target device only includes device select code of the ACK response of the Repeat start operation. In other words, if there are more than one Repeat Start operation, the target device includes device select of only the last Repeat Start from the Host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.
- NOTE 7 See [Figure 26](#) to see how target device ends the operation followed by Host STOP operation.
- NOTE 8 Repeat Start or Repeat Start with 7'h7E.

7.4.2 Read Operation - Data Packet (cont'd)

**Table 56 — Read Command Data Packet with IBI Header; No Pending IBI, PEC Enabled;
2 Byte Address Mode**

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|-------|---------------|-------|-------|-------|----------------|-------|-------|-------|------------------------|------|
| S | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^{[1],[2]} | |
| Sr | 1 | X | 0 | X | HID | | | W=0 | A ^{2,[3],[4]} | |
| | Address [7:0] | | | | | | | | T | |
| | CMD | | | R=1 | Address [11:8] | | | | T | |
| | PEC | | | | | | | | T | |
| Sr | 1 | X | 0 | X | HID | | | R=1 | A/N ^{[5],[6]} | |
| | Data | | | | | | | | T=1 | |
| | ... | | | | | | | | T=1 | |
| | Data | | | | | | | | T=1 | |
| | PEC | | | | | | | | T=0 ^[7] | |

NOTE 1 See [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Repeat Start).

NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 See [Figure 24](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 5 See [Figure 24](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 6 If PMIC device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If PMIC device NACKs due to PEC error or parity error, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the device may eventually ACK. The PEC calculation by the PMIC device only includes device select code of the ACK response of the Repeat Start operation. In other words, if there are more than one Repeat Start operation, the PMIC device includes device select of only the last Repeat Start from the host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.

NOTE 7 See [Figure 26](#) to see how Host ends target device operation followed by Host STOP operation.

NOTE 8 Repeat Start or Repeat Start with 7'h7E.

7.4.3 Default Read Address Pointer Mode

This mode works the same exact way as explained in Clause 7.3.3. [Table 57](#) and [Table 58](#) show the read command data packet for PEC function disabled and enabled respectively. When PEC function is enabled, [Table 163, Register 0x3A \[3:2\]](#) sets the number of bytes that PMIC device sends out followed by the PEC calculation. If PEC is enabled, the host must complete the burst length as indicated in [Table 163, Register 0x3A \[3:2\]](#) register. In other words, the host must not interrupt the burst length prematurely for default address pointer read operation.

7.4.3 Default Read Address Pointer Mode (cont'd)

Table 57 — Read Command Data Packet with Read Address Pointer Mode; PEC Disabled

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|------------------------|------------------------|
| S or Sr | 1 | X | 0 | X | HID | | | R=1 | A ^[1] | |
| | Data | | | | | | | | T=1 | |
| | ... | | | | | | | | T=1 | |
| | Data | | | | | | | | T=1 ^{[2],[3]} | Sr ^[4] or P |

- NOTE 1 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
- NOTE 2 See [Figure 25](#) to see how Host ends target device operation.
- NOTE 3 When PMIC device reaches last byte within the region (either Host region or DIMM vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for DIMM vendor region or Vendor specific region. Once the address counter reaches 0x1FF, it will reset to address 0x00 and it will continue to return the data. Only Host can perform STOP operation.
- NOTE 4 Repeat Start or Repeat Start with 7'h7E.

Table 58 — Read Command Data Packet with Read Address Pointer Mode; PEC Enabled

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|--------------------|------|
| S or Sr | 1 | X | 0 | X | HID | | | R=1 | A ^[1] | |
| | Data | | | | | | | | T=1 | |
| | ... | | | | | | | | T=1 | |
| | Data | | | | | | | | T=1 | |
| | PEC | | | | | | | | T=0 ^[2] | |

- NOTE 1 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
- NOTE 2 See [Figure 26](#) to see how target device ends the operation followed by STOP operation.
- NOTE 3 Repeat Start or Repeat Start with 7'h7E.

7.4.3 Default Read Address Pointer Mode (cont'd)

**Table 59 — Read Command Data Packet w/ Read Address Pointer and IBI Header;
No Pending IBI; PEC Disabled**

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|------------------------|------------------------|
| S | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^{[1],[2]} | |
| Sr | 1 | X | 0 | X | HID | | | R=1 | A/N ^{2,[3]} | |
| | Data | | | | | | | | T=1 | |
| | ... | | | | | | | | T=1 | |
| | Data | | | | | | | | T=1 ^{[4],[5]} | Sr ^[6] or P |

- NOTE 1 See [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
- NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
- NOTE 3 See [Figure 24](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
- NOTE 4 See [Figure 25](#) to see how Host ends target device operation.
- NOTE 5 When PMIC device reaches last byte within the region (either Host region or DIMM vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for DIMM vendor region or Vendor specific region. Once the address counter reaches 0x1FF, it will reset to address 0x00 and it will continue to return the data. Only Host can perform STOP operation.
- NOTE 6 Repeat Start or Repeat Start with 7'h7E.

**Table 60 — Read Command Data Packet with Read Address Pointer and IBI Header;
No Pending IBI; PEC Enabled**

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|----------------------|------|
| S | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^{[1],[2]} | |
| Sr | 1 | X | 0 | X | HID | | | R=1 | A/N ^{2,[3]} | |
| | Data | | | | | | | | T=1 | |
| | ... | | | | | | | | T=1 | |
| | Data | | | | | | | | T=1 | |
| | PEC | | | | | | | | T=0 ^[4] | |

- NOTE 1 See [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
- NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
- NOTE 3 See [Figure 24](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
- NOTE 4 See [Figure 26](#) to see how target device ends the operation followed by STOP operation.
- NOTE 5 Repeat Start or Repeat Start with 7'h7E.

7.4.3 Default Read Address Pointer Mode (cont'd)

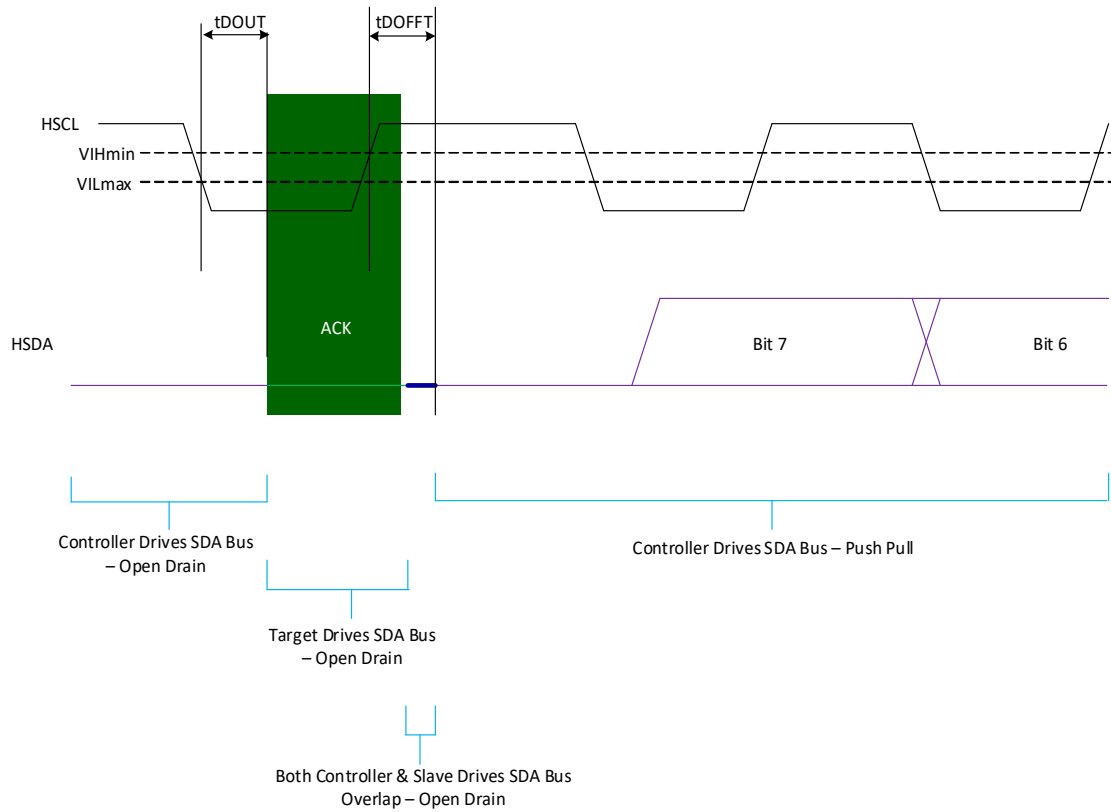


Figure 22 — Target Open Drain to Controller Push Pull Hand Off Operation

7.4.3 Default Read Address Pointer Mode (cont'd)

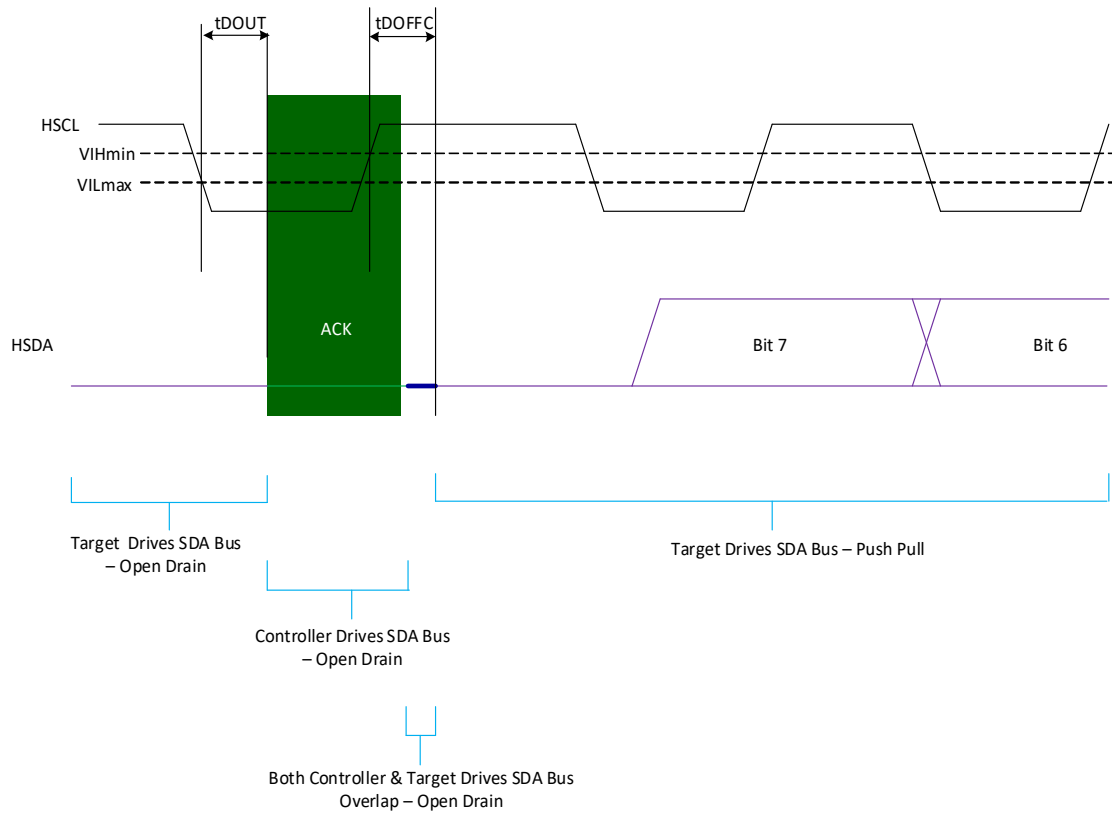


Figure 23 — Controller Open Drain (ACK) to Target Push Pull Hand Off Operation

7.4.3 Default Read Address Pointer Mode (cont'd)

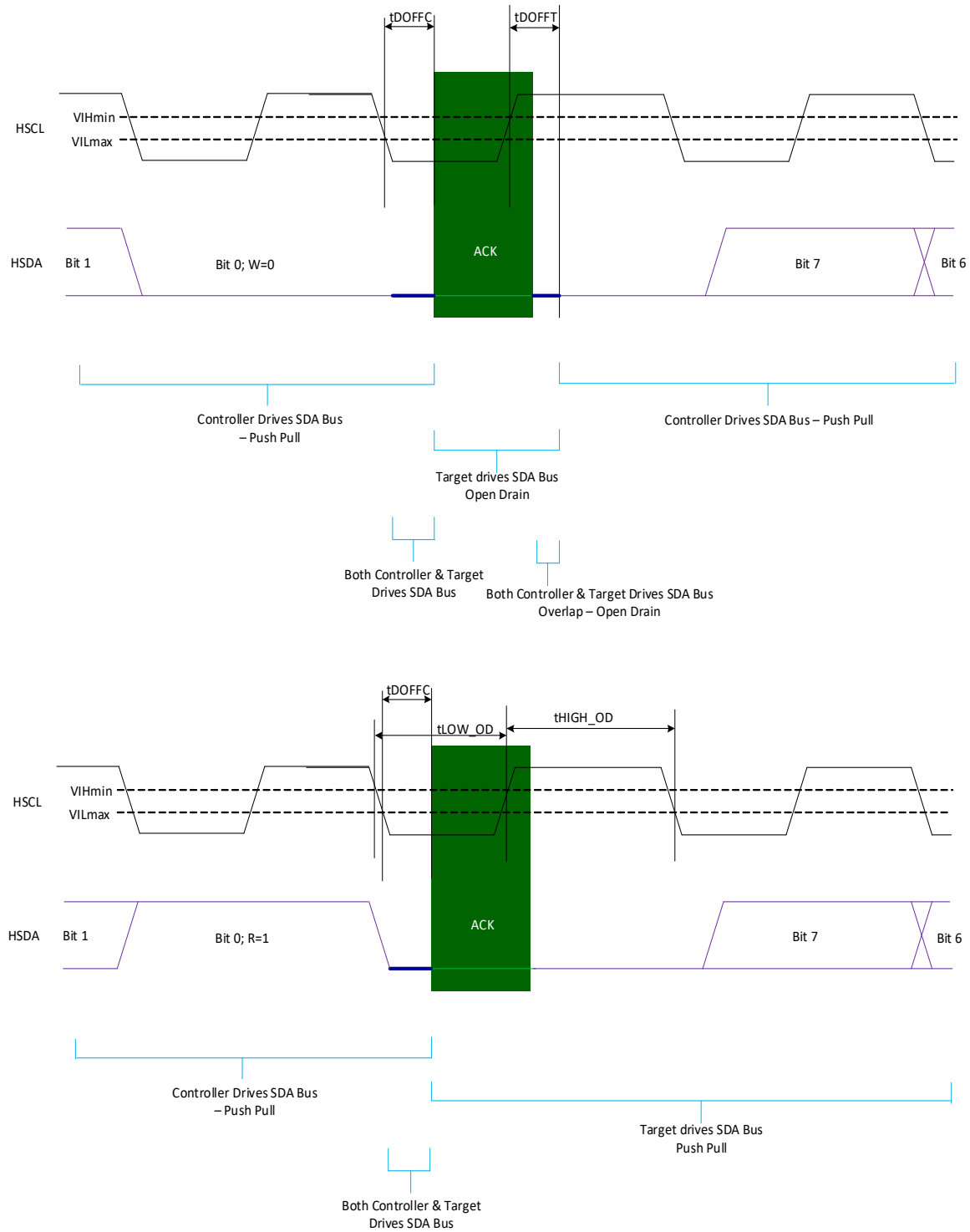


Figure 24 — Controller Push Pull to Target Open Drain Hand Off Operation

7.4.3 Default Read Address Pointer Mode (cont'd)

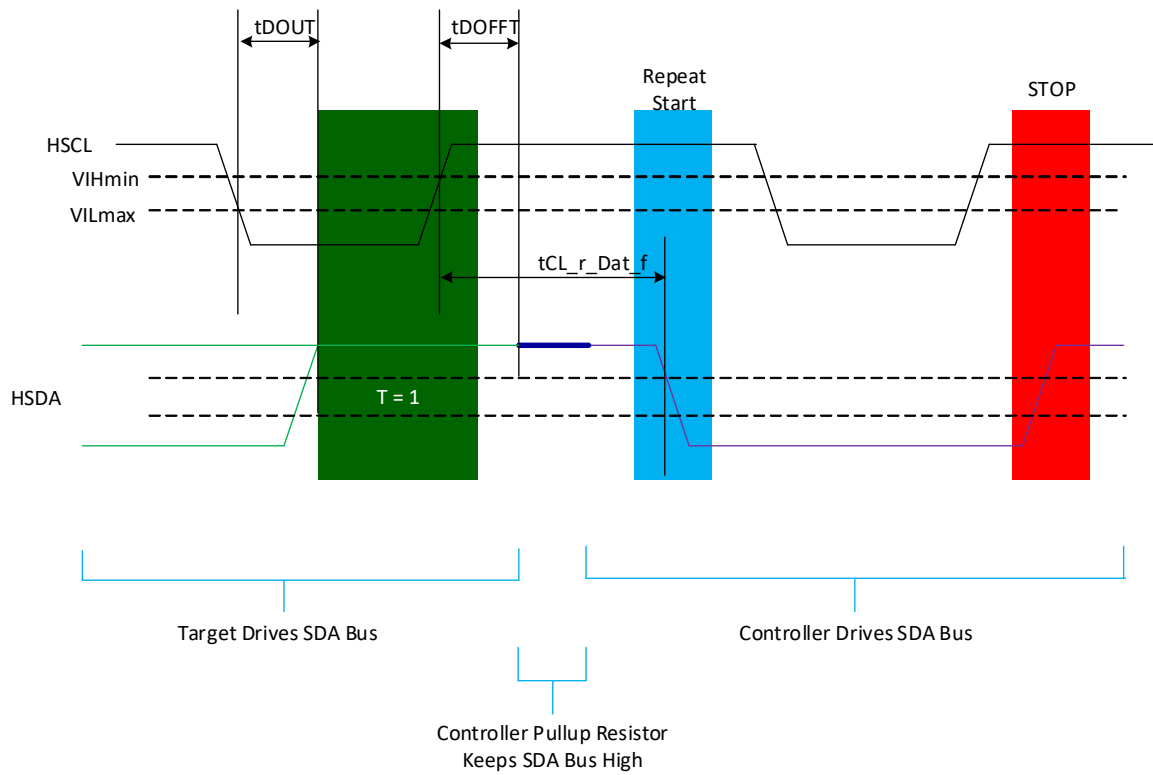


Figure 25 — T=1; Controller Ends Read with Repeated START and STOP Waveform

7.4.3 Default Read Address Pointer Mode (cont'd)

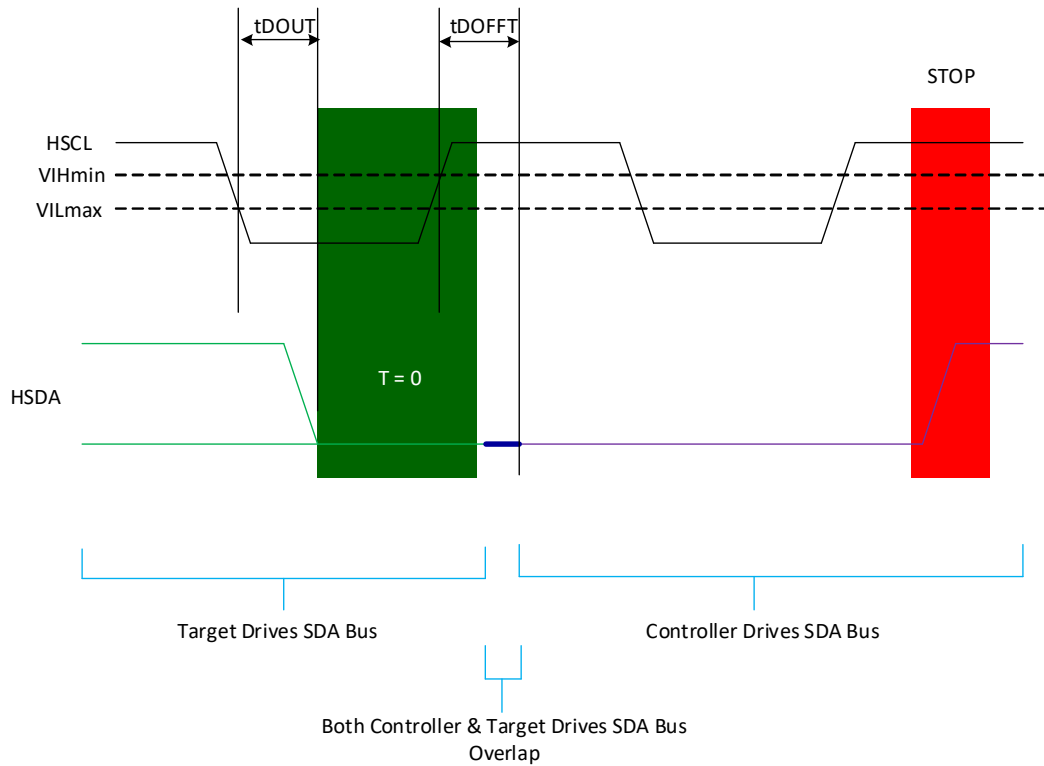


Figure 26 — T=0; Target Ends Read; Controller Generates STOP

7.5 In Band Interrupt (IBI)

In I²C mode, in band interrupt function is not supported. Only I³C Basic mode supports in band interrupt function.

7.5.1 Enabling and Disabling In Band Interrupt Function

By default, IBI function is disabled. The PMIC device enables the IBI when it registers ENEC CCC. Once enabled, the PMIC device sends an IBI when an event occurs.

- When [Table 158, Register 0x34 \[6\] = '1'](#), the device sends the IBI at next available opportunity when any of the register bits in [Table 113, Register 0x08 \[7:0\]](#), [Table 114, Register 0x09 \[7:0\]](#), [Table 115, Register 0x0A \[7:2\]](#), [Table 116, Register 0x0B \[7:0\]](#), [Table 157, Register 0x33 \[4:2\]](#), [Table 175, Register 0x108 \[7:0\]](#) and [Table 176, Register 0x109 \[7:0\]](#) is set to '1'. The device also sets [Table 115, Register 0x0A \[1\]](#) to '1' and updates Pending Interrupt Bits [3:0] = '0001' for GETSTATUS CCC.
- When [Table 158, Register 0x34 \[6\] = '0'](#), the device does not send the IBI regardless of the register bits in [Table 113, Register 0x08 \[7:0\]](#), [Table 114, Register 0x09 \[7:0\]](#), [Table 115, Register 0x0A \[7:2\]](#), [Table 116, Register 0x0B \[7:0\]](#), [Table 157, Register 0x33 \[4:2\]](#), [Table 175, Register 0x108 \[7:0\]](#) and [Table 176, Register 0x109 \[7:0\]](#). However, the device set [Table 115, Register 0x0A \[1\]](#) to '1' and updates Pending Interrupt Bits [3:0] = '0001' for GETSTATUS CCC.

7.5.2 Mechanics of Interrupt Generation

Event interrupts may be generated by the local device if IBI is enabled. When there is a pending interrupt (i.e., [Table 115, Register 0x0A \[1\] = '1'](#)) and if IBI is enabled (i.e., [Table 158, Register 0x34 \[6\] = '1'](#)) the PMIC device requests an interrupt after detecting START condition by transmitting its 7-bit binary address (LID bits followed by HID bits) followed by R/W = '1' on the SDA bus serially (synchronized by SCL falling transitions).

If PMIC device detects no START condition but if the I3C bus (SDA and SCL) has been inactive (no edges seen) for t_{AVAL} period, then PMIC device may assert SDA low by t_{IBI_ISSUE} time to request an interrupt. When the PMIC device requests an interrupt, the Host toggles the SCL. The PMIC device transmits its 7-bit binary address (LID bits followed by HID bits) followed by R/W bit = '1' to the Host.

When the PMIC device requests an interrupt, the host may take one of the two actions below.

- The Host sends ACK on 9th bit to accept the interrupt request. At this point, if the PMIC device confirms that it has won the arbitration, the PMIC device transmits the IBI payload as shown in [Table 61](#) and [Table 62](#) for PEC disabled and PEC enabled configuration respectively. See [Figure 27](#). [Figure 27](#) just shows only first two data bits of the MDB byte to illustrate the timing. The interrupt payload contains MDB followed by [Table 113, Register 0x08](#), [Table 114, Register 0x09](#), [Table 115, Register 0x0A](#), [Table 116, Register 0x0B](#), [Table 157, Register 0x33](#), [Table 175, Register 0x108](#) and [Table 176, Register 0x109](#) bytes. The host then issues the STOP command. Note the timing waveform in [Figure 27](#). The host then accepts the IBI payload if it sends an ACK on 9th bit to accept the interrupt request. The host can interrupt the IBI payload at T bit. If host stops the IBI payload at T bit in the middle of payload, the PMIC retains the IBI status flag ([Table 115, Register 0x0A \[1\]](#)) and Pending Interrupt Bits [3:0] internally and waits for the next opportunity to request an interrupt. If the PMIC device successfully transmits the entire IBI payload, it then clears IBI status flag ([Table 115, Register 0x0A \[1\] = '0'](#)) and Pending Interrupt Bits [3:0] = '0000' on its own and does not request for an IBI again unless there is another different event occurs; for another same event, the device does not request for an IBI.
- The Host sends NACK on the 9th bit as shown in [Figure 28](#) followed by a STOP command. In this case, the PMIC device does not transmit the IBI payload and waits for the next opportunity to request an interrupt. At this point, though Host sent an NACK, it does have a knowledge of which PMIC device sent the IBI request. The PMIC device retains the IBI status flag ([Table 115, Register 0x0A \[1\] = '1'](#)) and Pending Interrupt Bits [3:0] = '0001'.

7.5.2 Mechanics of Interrupt Generation (cont'd)

Table 61 — Target Device IBI Payload Packet; PEC is Disabled

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/T | Stop |
|-------|------------|-------|-------|-------|-------|-------|-------|-------|--------------------|------|
| S | 1 | X | 0 | X | HID | | | R=1 | A ^[1] | |
| | MDB = 0x00 | | | | | | | | T=1 | |
| | R08 [7:0] | | | | | | | | T=1 | |
| | R09 [7:0] | | | | | | | | T=1 | |
| | R0A [7:0] | | | | | | | | T=1 | |
| | R0B [7:0] | | | | | | | | T=1 | |
| | R33 [7:0] | | | | | | | | T=1 | |
| | R108 [7:0] | | | | | | | | T=1 | |
| | R109 [7:0] | | | | | | | | T=0 ^[2] | P |

NOTE 1 See [Figure 23](#) to see how the transition occurs from Host Open Drain (ACK) to Target Push Pull Operation (1st bit of MDB Byte bit [7]).

NOTE 2 See [Figure 26](#) to see how target device ends the operation followed by Host STOP operation.

Table 62 — Target Device IBI Payload Packet; PEC is Enabled

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/T | Stop |
|-------|------------|-------|-------|-------|-------|-------|-------|-------|--------------------|------|
| S | 1 | X | 0 | X | HID | | | R=1 | A ^[1] | |
| | MDB 0x00 | | | | | | | | T=1 | |
| | R08 [7:0] | | | | | | | | T=1 | |
| | R09 [7:0] | | | | | | | | T=1 | |
| | R0A [7:0] | | | | | | | | T=1 | |
| | R0B [7:0] | | | | | | | | T=1 | |
| | R33 [7:0] | | | | | | | | T=1 | |
| | R108 [7:0] | | | | | | | | T=1 | |
| | R109 [7:0] | | | | | | | | T=1 | |
| | PEC | | | | | | | | T=0 ^[2] | P |

NOTE 1 See [Figure 23](#) to see how the transition occurs from Host Open Drain (ACK) to Target Push Pull Operation (1st bit of MDB Byte bit [7]).

NOTE 2 See [Figure 26](#) to see how target device ends the operation followed by Host STOP operation.

7.5.2 Mechanics of Interrupt Generation (cont'd)

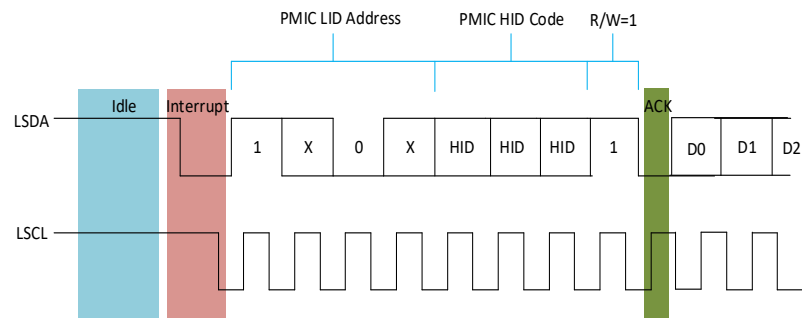


Figure 27 — PMIC Requests Interrupt, Host ACK followed by PMIC Device IBI Payload

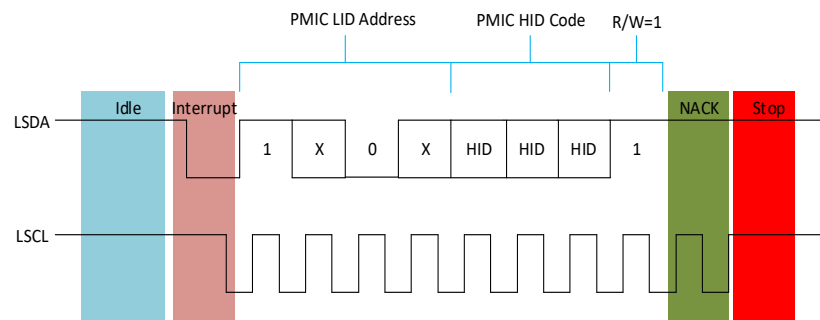


Figure 28 — PMIC Requests Interrupt; Host NACK followed by STOP

7.5.3 Interrupt Arbitration

As there are multiple devices I3C Basic bus, multiple device may request an interrupt when the Host I3C Basic bus is inactive for t_{AVAL} period. Arbitration process is required.

For DDR5 DIMM application environment, there could be up to total of 13 difference devices including the PMIC on I3C bus.

On a typical DDR5 DIMM application environment, all devices have the same 3-bit HID code. Hence the arbitration is always won by the lowest 4-bit LID code. For example, if one target device has LID code of '0010' and other device (PMIC) has a LID code of '1001', through the arbitration process, the target device LID code of '0010' wins. The PMIC device with a LID code of '1001' must release the bus and wait for next opportunity to request an interrupt. Table 63 shows the arbitration priority based on the LID code for all devices. The Green color cells in Table 63 are the likely devices that will be on a standard DDR5 RDIMM or DDR5 LRDIMM. The Olive color cells in Table 63 do not apply.

7.5.3 Interrupt Arbitration (cont'd)

Table 63 — Interrupt Arbitration - Among All Devices

| Device | LID Code | HID Code = '111' | Arbitration Priority |
|---------|----------|------------------|----------------------|
| N/A | 0000 | N/A | N/A |
| RFU | 0001 | 111 | 1 |
| TS0 | 0010 | 111 | 2 |
| RFU | 0011 | 111 | 3 |
| RFU | 0100 | 111 | 4 |
| RFU | 0101 | 111 | 5 |
| TS1 | 0110 | 111 | 6 |
| RFU | 0111 | 111 | 7 |
| PMIC1 | 1000 | 111 | 8 |
| PMIC0 | 1001 | 111 | 9 |
| SPD Hub | 1010 | N/A | N/A |
| RCD | 1011 | 111 | 10 |
| PMIC2 | 1100 | 111 | 11 |
| RFU | 1101 | 111 | 12 |
| RFU | 1110 | 111 | 13 |
| N/A | 1111 | N/A | N/A |

In an uncommon but possible scenario would be that at the exact same time as when the Hub or local target devices (i.e., PMIC) are requesting an interrupt, the host is starting an operation to the Hub or local target devices (i.e., PMIC). When this happens, Host also gets involved in the arbitration process along with the Hub or the local target devices (PMIC). During the arbitration phase, there will be always only one winning device and it could be either Hub or the local target device (i.e., PMIC) or the Host.

If the host wins during the arbitration phase, it continues with normal operation. The losing Hub or local target device (i.e., PMIC) waits for next opportunity to send an interrupt.

If the host loses during the arbitration phase, it host must let go of the bus. When Host loses during the arbitration, the host must let the Hub or local target device (i.e., PMIC) finish sending their 4-bit LID code followed by 3-bit HID code followed by R/W = '1'. At this point, during the 9th bit, the host has two options to take the action as noted below:

Host sends an ACK to accept the interrupt and hence accepts the IBI payload from the winning Hub or local target device (i.e., PMIC). After the IBI payload, the host issues STOP operation.

Host sends an NACK followed by STOP operation.

In a rare but still possible scenario would be that at the exact same time as when the PMIC is requesting an interrupt, the host is starting an operation to the same PMIC. When this happens, neither Host nor the PMIC knows it is a winner until the 8th bit and Host always wins. This is because; the PMIC sends R=1 (8th bit) during the interrupt. The host sets W=0 (8th bit) during the operation. As a result, the host wins and the PMIC must let go of the bus and wait for the next opportunity to send an interrupt.

7.5.3 Interrupt Arbitration (cont'd)

In an extremely rare but still possible scenario would be that at the same exact time as when PMIC device is requesting an interrupt, the host is requesting a read operation with the default read address pointer mode to the PMIC device. When this happens, there is no winning device. This is the only time there is no winning device. This is because, the PMIC device sends R=1 (8th bit) during the interrupt and Host also sends R=1 for read request with default read address pointer mode. As a result, there is no winner because Host is waiting for PMIC to ACK and PMIC is waiting for Host to ACK. In this case, neither Host nor PMIC will ACK. Since there is no ACK (i.e., NACK) by either device, the Host must time out and repeat the read request with Repeat Start. When Host repeats the read request with Repeat Start, the PMIC does not send an interrupt because of Repeat Start.

7.5.4 Clearing Device Status and IBI Status Registers

The PMIC device provides the IBI status in [Table 115, Register 0x0A \[1\]](#) by setting it to '1'. The PMIC device clears the IBI status register [Table 115, Register 0x0A \[1\]](#) to '0' automatically when it sends a complete IBI (including payload and without interruption) and it also clears Pending Interrupt Bits [3:0] to '0000'. Once IBI status register is cleared, the PMIC does not request for an IBI again unless another event occurs.

The PMIC device provides the device status in [Table 113, Register 0x08 \[7:0\]](#), [Table 114, Register 0x09 \[7:0\]](#), [Table 115, Register 0x0A \[7:2\]](#), [Table 116, Register 0x0B \[7:0\]](#) and [Table 157, Register 0x33 \[4:2\]](#) registers. The status information in [Table 113, Register 0x08 \[7:0\]](#), [Table 114, Register 0x09 \[7:0\]](#), [Table 115, Register 0x0A \[7:2\]](#), [Table 116, Register 0x0B \[7:0\]](#) and [Table 157, Register 0x33 \[4:2\]](#) registers are latched and remains set even after the PMIC device sends IBI payload and clears the IBI status register [Table 115, Register 0x0A \[1\]](#) to '0'. The host must explicitly clear the status register through Clear command by writing '1' for appropriate status or by issuing a Global clear command.

After Host issues clear command, if the condition is no longer present, the PMIC device clears the appropriate status register, clears the IBI status register [Table 115, Register 0x0A \[1\]](#) to '0' and Pending Interrupt Bits [3:0] to '0000' even if the PMIC device has not sent the IBI. After Host issues clear command, if the condition is still present, the device will again set the appropriate status register, sets the IBI status register [Table 115, Register 0x0A \[1\]](#) to '1' and Pending Interrupt Bits [3:0] to '0001' even if the device has already sent the IBI and entire IBI payload.

7.5.5 Packet Error Check (PEC) Function

In I²C mode, packet error checking is not supported. Only I3C Basic mode supports packet error checking.

The PMIC device implements an 8-bit Packet Error Code (PEC) which is appended at the end of all transactions if PECs is enabled through DEVCTRL CCC. The PEC is a CRC-8 value calculated on all the messages bytes except for START, STOP, REPEATED START conditions or T-bits, ACK and NACK and IBI header (7'h7E followed W=0) bits.

The polynomial for CRC-8 calculations is:

$$C(X) = X^8 + X^2 + X^1 + 1$$

The seed value for PEC function is all zero.

When Host calculates PEC for PMIC device, it includes LID and HID bits followed by R/W bit.

7.5.6 Parity Error Check Function

In I²C mode, parity error checking is not supported except for supported CCCs. Only I3C Basic mode supports parity error checking.

By default, when PMIC device is put in I3C Basic mode, parity function is automatically enabled. The host can disable the function after it is enabled. Host can also disable the parity function with DEVCTRL CCC. When parity function is disabled, the PMIC device simply ignores the “T” bit information from the Host. The host may actually choose to compute the parity and send that information during “T” bit or simply drive static low or high in “T” bit.

The PMIC device implements ODD parity. If an odd number of bits in the byte are ‘1’, the parity bit value is ‘0’. If even number of bits in the byte are ‘1’, the parity bit value is ‘1’. The host computes the parity and sends during “T” bit.

7.5.7 Packet Error Check and Parity Error Handling

There are two types of error checking done by the PMIC device. Parity error checking and Packet Error checking. By default, the parity error checking is always enabled and packet error checking is disabled. The host may enable the packet error checking at any time. The parity error is checked for each byte in a packet except for the device select code byte from the host. The host sends parity error information in “T” bit.

I3C Basic defines TE0, TE1, TE2, TE3, TE4, TE5, and TE6 error detections for target devices. Only TE1 and TE2 error detections are supported by the PMIC for parity checking. All other errors are not supported and not applicable.

7.5.7.1 Write Command Data Packet Error Handling - PEC Disabled

The PMIC device checks for the parity error for each byte in a packet that it receives from the host except for the device select code byte that it receives from the host as shown in [Table 64](#).

Table 64 — Write Command Data Packet; PEC Disabled; 1 Byte Address Mode

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|---------------|-------|-------|-------|-------|-------|-------|-------|--------------------------|------------------------|
| S or Sr | 1 | X | 0 | X | HID | | | W=0 | A ^{[1],[2],[3]} | |
| | Address [7:0] | | | | | | | | T | |
| | Data | | | | | | | | T | |
| | ... | | | | | | | | T | |
| | Data | | | | | | | | T | Sr ^[4] or P |

NOTE 1 See [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit [7]).

NOTE 2 The PMIC NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC does not check for parity error in subsequent bytes when it determines the 7-bit device select code issues by the host does not match with its own device code. The PMIC ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 Repeat Start or Repeat Start with 7'h7E.

Write command - if no parity error:

- The PMIC device executes the command.

7.5.7.1 Write Command Data Packet Error Handling - PEC Disabled (cont'd)

Write command - if parity error:

- The PMIC device discards the byte in the packet that had a parity error.
- The PMIC device discards all subsequent bytes in that packet until the STOP operation. The PMIC device may or may not check parity for all sub-sequent bytes in that packet.
- Note that as the packet contains more than one byte, if first byte had no parity error but the second byte had a parity error, the PMIC device may or may not execute the first byte operation but second byte and all subsequent bytes operations are discarded.
- The PMIC device sets the [Table 115, Register 0x0A \[2:1\]](#) to '11'; P_Err in GETSTATUS CCC to '1'; updates Pending Interrupt Bits [3:0] in GETSTATUS CCC to '0001'; asserts GSI_n pin if enabled and waits for the next opportunity to send an in band interrupt if IBI is enabled.

7.5.7.2 Read Command Data Packet Error Handling - PEC Disabled

The PMIC device checks for parity error for each byte in a packet except for the device select code byte that it receives from the host prior to Repeat Start as shown in [Table 65](#).

The PMIC device does not compute the parity when it sends the data to the Host. The Host does not check for parity error for the bytes shown in [Table 65](#). The device sends Continuous ('1') or Stop ('0') information during "T" bit when PMIC device is sending the read data.

Table 65 — Read Command Data Packet; PEC Disabled; 1 Byte Address Mode

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|---------------|-------|-------|-------|-------|-------|-------|-------|--------------------------|------------------------|
| S or Sr | 1 | X | 0 | X | HID | | | W=0 | A ^{[1],[2],[3]} | |
| | Address [7:0] | | | | | | | | T | |
| Sr | 1 | X | 0 | X | HID | | | R=1 | A/N ^{[4],[5]} | |
| | Data | | | | | | | | T=1 | |
| | ... | | | | | | | | T=1 | |
| | Data | | | | | | | | T=1 ^{[6],[7]} | Sr ^[8] or P |

NOTE 1 See [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit [7]).

NOTE 2 The PMIC NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC does not check for parity error in subsequent bytes when it determines the 7-bit device select code issues by the host does not match with its own device code. The PMIC ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 If target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If target device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity errors, the PMIC may eventually ACK.

NOTE 5 See [Figure 24](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 6 See [Figure 25](#) to see how Host ends target device operation.

NOTE 7 When PMIC device reaches last byte within the region (either Host region or DIMM vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for DIMM vendor region or Vendor specific region. Once the address counter reaches the address 0x1FF, it will reset to address 0x00 and it will continue to return the data. Only Host can perform STOP operation.

NOTE 8 Repeat Start or Repeat Start with 7'h7E.

7.5.7.2 Read Command Data Packet Error Handling - PEC Disabled (cont'd)

Read Command - If no parity error:

- The PMIC sends ACK back to the host when Host performs Repeat Start operation.
- The PMIC device executes the command and sends the data as shown in Table 65.

Read Command - If parity error:

- The PMIC device discards the byte in the packet that had a parity error.
- The PMIC device sends NACK back to the host when Host performs a Repeat Start operation. This is shown in the RED color cell in Table 65. The NACK represents either a parity error in one of the two bytes or that PMIC is not able to start the read operation. The host may re-try Repeat Start again. The host may do the Repeat Start as many times as it may desire. If the PMIC target device NACKs due to parity error in a previous byte from the host, it will always NACK regardless of how many times Host tries Repeat Start.
- The PMIC does not send the data shown in Table 65 and instead expects Host to perform STOP operation.
- The PMIC device sets Table 115, Register 0x0A [2:1] to '11'; P_Err in GETSTATUS CCC to '1'; updates Pending Interrupt Bits [3:0] in GETSTATUS CCC to '0001'; asserts GSI_n pin if enabled and waits for the next opportunity to send an in band interrupt if IBI is enabled.

7.5.7.3 Write Command Data Packet Error Handling - PEC Is Enabled

The PMIC device checks for the parity error for each byte in a packet that it receives from the host except for the device select code byte that it receives from the host as shown in Table 66. Further, the PMIC device checks for the packet error for the entire packet (from Start condition until last byte of Data) that it receives from the host as shown in Table 66.

Table 66 — Write Command Data Packet; PEC Enabled; 1 Byte Address Mode

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|---------------|-------|-------|-------|-------|-------|-------|-------|--------------------------|------------------------|
| S or Sr | 1 | X | 0 | X | HID | | | W=0 | A ^{[1],[2],[3]} | |
| | Address [7:0] | | | | | | | | T | |
| | CMD | | | W=0 | 0 | 0 | 0 | 0 | T | |
| | Data | | | | | | | | T | |
| | ... | | | | | | | | T | |
| | Data | | | | | | | | T | |
| | PEC | | | | | | | | T | Sr ^[4] or P |

NOTE 1 See Figure 22 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Address bit 7).

NOTE 2 The PMIC NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issues by the host does not match with its own device code. The PMIC ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 Repeat Start or Repeat Start with 7'h7E.

7.5.7.3 Write Command Data Packet Error Handling - PEC Is Enabled (cont'd)

Write command - if no parity error:

- The PMIC device waits for the entire packet. If no error in packet, the PMIC device executes the command. If there is an error in the packet, the PMIC device discards the entire packet and does not execute the packet and waits for STOP; sets the [Table 115, Register 0x0A](#) [3,1] to '11'; PEC_Err in GETSTATUS CCC to '1'; updates Pending Interrupt Bits [3:0] in GETSTATUS CCC to '0001'; asserts GSI_n pin if enabled and waits for the next opportunity to send an in band interrupt if IBI is enabled.

Write command - if parity error:

- The PMIC device discards that byte and the entire packet until STOP operation.
- The PMIC device sets the [Table 115, Register 0x0A](#) [2:1] to '11'; P_Err in GETSTATUS CCC to '1'; updates Pending Interrupt Bits [3:0] in GETSTATUS CCC to '0001'; asserts GSI_n pin if enabled and waits for the next opportunity to send an in band interrupt if IBI is enabled.
- The PMIC device may or may not check the error for the packet. If the PMIC device checks for the packet error, likely it will detect an error in the packet and the device may also set [Table 115, Register 0x0A](#) [3] and PEC_Err in GETSTATUS CCC as well.

7.5.7.4 Read Command Data Packet Error Handling - PEC Is Enabled

The PMIC device checks for parity error for each byte in a packet except for the device select code byte that it receives from the host prior to Repeat Start as shown in [Table 67](#).

The PMIC device does not compute the parity when it sends the data to the Host. The Host does not check for parity error for the bytes shown in [Table 67](#). The device sends Continuous ('1') or Stop ('0') information during "T" bit when PMIC device is sending the read data.

The PMIC device checks for the PEC error in a packet that it receives from Host from Start condition to Repeat Start (from first device select code followed by the address offset and CMD byte).

The PMIC device computes the packet error code for the entire packet starting with Repeat Start (device select code and the data PMIC device transmits back to Host).

Table 67 — Read Command Data Packet; PEC Enabled; 1 Byte Address Mode

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|---------------|-------|-------|-------|-------|-------|-------|-------|--------------------------|------------------------|
| S or Sr | 1 | X | 0 | X | HID | | | W=0 | A ^{[1],[2],[3]} | |
| | Address [7:0] | | | | | | | | T | |
| | CMD | | | R=1 | 0 | 0 | 0 | 0 | T | |
| | PEC | | | | | | | | T | |
| Sr | 1 | X | 0 | X | HID | | | R=1 | A/N ^{[4],[5]} | |
| | Data | | | | | | | | T=1 | |
| | ... | | | | | | | | T=1 | |
| | Data | | | | | | | | T=1 | |
| | PEC | | | | | | | | T=0 ^[6] | Sr ^[7] or P |

- NOTE 1 See [Figure 22](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Address bit 7).
- NOTE 2 The PMIC NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
- NOTE 3 The PMIC does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issues by the host does not match with its own device code. The PMIC ignores the entire packet until STOP or next Repeat Start operation.
- NOTE 4 If target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If target device NACKs due to PEC error or parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the PMIC may eventually ACK. The PEC calculation by the target device only includes device select code of the ACK response of the Repeat start operation. In other words, if there are more than one Repeat Start operation, the target device includes device select of only the last Repeat Start from the Host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.
- NOTE 5 See [Figure 24](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
- NOTE 6 See [Figure 26](#) to see how target device ends the operation followed by Host STOP operation.
- NOTE 7 Repeat Start or Repeat Start with 7'h7E.

Read command - If no parity error and no PEC error

- The PMIC device sends ACK back to the host when Host performs a Repeat Start operation.
- The PMIC device executes the command and sends the data as shown in [Table 67](#).
- The PMIC computes PEC for the bytes (from Start condition to PEC byte prior to Repeat Start) shown in the cells in [Table 67](#).

Read command - if parity error or PEC error

- The PMIC device discards the byte in the packet that had a parity error.
- The PMIC device discards second byte in that packet if a parity error occurred in first byte. The PMIC device may or may not check parity for the second byte in that packet.
- The PMIC device discards the packet if there is a PEC error.
- The PMIC sends NACK back to the host when Host performs Repeat Start operation. This is shown in the **RED color** cell in [Table 67](#). The NACK represents either PEC error or a parity error in one of the three bytes or that PMIC is not able to start the read operation. The host may re-try Repeat Start again. The host may do the Repeat Start as many times it may desire. The PEC calculation by PMIC device only includes device select code of the ACK responses of the Repeat Start operation. In other words, if there are more than one Repeat Start operation, the PMIC device includes the device select of only the last Repeat Start from the Host when it ACKs in PEC calculation and other NACK responses of the device select codes of the Repeat Start are not included in PEC calculation. If the PMIC target device NACKs due to PEC error or a parity error in a previous bytes from Host, it will always NACK regardless of how many times Host tries Repeat Start.
- The PMIC device does not send any data shown in [Table 67](#) and instead expects Host to perform STOP operation.
- The PMIC device sets [Table 115, Register 0x0A \[3:2\]](#) accordingly and [Table 115, Register 0x0A \[1\]](#) to '1'; P_Err, PEC_Err in GETSTATUS CCC to '1' accordingly; updates Pending Interrupt Bits [3:0] in GETSTATUS CCC to '0001'; asserts GSI_n pin if enabled and waits for the next opportunity to send an in band interrupt if IBI is enabled.

7.5.8 CCC Packet Error Handling

Parity error and PEC error detected in a CCC packet are handled the same way as described for normal Read/Write operations.

7.5.9 Error Reporting

All error conditions detected by the PMIC devices are captured in [Table 113, Register 0x08 \[7:0\]](#), [Table 114, Register 0x09 \[7:0\]](#), [Table 115, Register 0x0A \[7:1\]](#), [Table 116, Register 0x0B \[7:0\]](#), [Table 157, Register 0x33 \[4:2\]](#), [Table 175, Register 0x108 \[7:0\]](#) and [Table 176, Register 0x109 \[7:6,0\]](#) registers.

There are four different possible ways error information can be communicated to the host.

1. The host makes the read request to [Table 113, Register 0x08](#), [Table 114, Register 0x09](#), [Table 115, Register 0x0A](#), [Table 116, Register 0x0B](#), [Table 157, Register 0x33](#), [Table 175, Register 0x108](#) and [Table 176, Register 0x109](#) registers.
2. The host starts any transactions with Start condition followed by 7'h7E IBI header, if IBI is enabled (Only applicable in I3C Basic mode).
3. The PMIC device sends in band interrupt if enabled, when its SCL and SDA input has been idle for t_{AVAL} time (Only applicable in I3C Basic mode).
4. The PMIC device asserts GSI_n pin if enabled.

7.5.10 I3C Basic Common Command Codes (CCC)

The I3C Basic spec lists large number of Common Command Codes (CCC). Not all CCC are required to be supported. The PMIC device NACKs for all unsupported CCC. The PMIC supports CCC as listed in [Table 68](#).

The PMIC device requires STOP operation in between when switching from CCC operation to private device specific Write or Read or Default Read Address Pointer mode operation and vice versa. In other words, any CCC operation must be followed by STOP operation before continuing to any device specific Write or Read or Default Read Address Pointer mode operation. Similarly, any device specific Write or Read or Default Read Address Pointer mode operation must be followed by STOP operation before continuing to any CCC operation. The PMIC device also requires STOP operation between any direct CCC to broadcast CCC.

The PMIC device does allow Repeat Start operation between any direct CCC to any other direct CCC or between any broadcast CCC to any other broadcast CCC or between any private Write or Read or Default Read Address Pointer mode operation to any other private Write or Read or Default Read Address Pointer mode operation.

7.5.10 I3C Basic Common Command Codes (CCC) (cont'd)

Table 68 — PMIC CCC Support Requirement

| CCC | Mode | Code | Description | Note |
|-----------|-----------|------|---|------|
| ENEC | Broadcast | 0x00 | Enable Event Interrupts | |
| | Direct | 0x80 | | |
| DISEC | Broadcast | 0x01 | Disable Event Interrupts | |
| | Direct | 0x81 | | |
| RSTDAA | Broadcast | 0x06 | Put the device in I ² C Mode (aka: Reset Dynamic Address Assignment) | |
| SETAASA | Broadcast | 0x29 | Put the device in I3C Basic Mode (aka: Set All Addresses to Static Address) | |
| GETSTATUS | Direct | 0x90 | Get Device Status | |
| DEVCAP | Direct | 0xE0 | Get Device Capability | [1] |
| SETHID | Broadcast | 0x61 | PMIC updates 3-bit HID field | 1 |
| DEVCTRL | Broadcast | 0x62 | Configure SPD Hub and all devices behind Hub | 1 |

NOTE 1 JEDEC-specific CCC.

7.5.10.1 ENEC CCC

The ENEC CCC is only supported after device is put in I3C Basic mode. In I²C mode, it is illegal for host to issue this CCC; the PMIC may ignore it or subsequent PMIC operation may not be guaranteed and the PMIC may require Bus Reset. When ENEC CCC is registered by the PMIC, it updates [Table 158, Register 0x34](#) [6] = '1' and it takes in effect at the next Start operation (i.e., after STOP operation). [Table 69](#) through [Table 72](#) show an example of a single ENEC CCC. [Table 73](#) shows the encoding definition for ENEC CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 69 — ENEC CCC - Broadcast

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|------------------|-------|-------|-------|-------|-------|-------|-------|------------------|------------------------|
| S or Sr | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^[1] | |
| | 0x00 (Broadcast) | | | | | | | | T | |
| | 0x00 | | | | | | | ENINT | T | Sr ^[2] or P |

NOTE 1 The PMIC NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 Repeat Start or Repeat Start with 7'h7E.

7.5.10.1 ENEC CCC (cont'd)**Table 70 — ENEC CCC - Broadcast with PEC**

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|------------------|-------|-------|-------|-------|-------|-------|-------|------------------|------------------------|
| S or Sr | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^[1] | |
| | 0x00 (Broadcast) | | | | | | | | T | |
| | 0x00 | | | | | | | ENINT | T | |
| | PEC | | | | | | | | T | |
| | | | | | | | | | | Sr ^[2] or P |

NOTE 1 The PMIC NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 Repeat Start or Repeat Start with 7'h7E.

Table 71 — ENEC CCC - Direct

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|---------------|-------|-------|-------|-------|-------|-------|-------|--------------------|------------------------|
| S or Sr | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^[1] | |
| | 0x80 (Direct) | | | | | | | | T | |
| Sr | DevID[6:0] | | | | | | | W=0 | A ^{1,[2]} | |
| | 0x00 | | | | | | | ENINT | T | |
| | | | | | | | | | | Sr ^[3] or P |

NOTE 1 The PMIC NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 The PMIC device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The PMIC device ignores the entire packet until STOP operation or next Repeat Start operation.

NOTE 3 Repeat Start or Repeat Start with 7'h7E.

Table 72 — ENEC CCC - Direct with PEC

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|---------------|-------|-------|-------|-------|-------|-------|-------|--------------------|------------------------|
| S or Sr | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^[1] | |
| | 0x80 (Direct) | | | | | | | | T | |
| | PEC | | | | | | | | T | |
| Sr | DevID[6:0] | | | | | | | W=0 | A ^{1,[2]} | |
| | 0x00 | | | | | | | ENINT | T | |
| | PEC | | | | | | | | T | |
| | | | | | | | | | | Sr ^[3] or P |

NOTE 1 The PMIC NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 The PMIC device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The PMIC device ignores the entire packet until STOP operation or next Repeat Start operation.

NOTE 3 Repeat Start or Repeat Start with 7'h7E.

7.5.10.1 ENEC CCC (cont'd)

Table 73 — ENEC CCC Byte Encoding

| Bit | Encoding | Notes |
|-------|---|---|
| ENINT | 0 = No Action 1 = Enable IBI Interrupt | It is illegal for Host to issue ENEC CCC with ENINT bit = '0'; the PMIC may ignore it or subsequent PMIC operation may not be guaranteed and the PMIC may require Bus Reset |

7.5.10.2 DISEC CCC

The DISEC CCC is only supported after device is put in I3C Basic mode. In I²C mode, it is illegal for host to issue this CCC; the PMIC may ignore it or subsequent PMIC operation may not be guaranteed and the PMIC may require Bus Reset. When DISEC CCC is registered by the PMIC, it updates [Table 158, Register 0x34](#) [6] = '0' and it takes in effect at the next Start operation (i.e., after STOP operation). [Table 74](#) through [Table 77](#) show an example of a single DISEC CCC. [Table 78](#) shows the encoding definition for DISEC CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 74 — DISEC CCC - Broadcast

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|------------------|-------|-------|-------|-------|-------|-------|--------|------------------|------------------------|
| S or Sr | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^[1] | |
| | 0x01 (Broadcast) | | | | | | | | T | |
| | 7'h00 | | | | | | | DISINT | T | Sr ^[2] or P |

NOTE 1 The PMIC NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 Repeat Start or Repeat Start with 7'h7E.

Table 75 — DISEC CCC - Broadcast with PEC

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|------------------|-------|-------|-------|-------|-------|-------|--------|------------------|------------------------|
| S or Sr | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^[1] | |
| | 0x01 (Broadcast) | | | | | | | | T | |
| | 7'h00 | | | | | | | DISINT | T | |
| | PEC | | | | | | | | T | Sr ^[2] or P |

NOTE 1 The PMIC NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 Repeat Start or Repeat Start with 7'h7E.

7.5.10.2 DISEC CCC (cont'd)**Table 76 — DISEC CCC - Direct**

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|---------------|-------|-------|-------|-------|-------|-------|--------|--------------------|------|
| S or Sr | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^[1] | |
| | 0x81 (Direct) | | | | | | | | T | |
| Sr | DevID[6:0] | | | | | | | W=0 | A ^{1,[2]} | |
| | 0x00 | | | | | | | DISINT | T | |

- NOTE 1 The PMIC NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
- NOTE 2 The PMIC device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The PMIC device ignores the entire packet until STOP operation or next Repeat Start operation.
- NOTE 3 Repeat Start or Repeat Start with 7'h7E.

Table 77 — DISEC CCC - Direct with PEC

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|---------------|-------|-------|-------|-------|-------|-------|--------|--------------------|------|
| S or Sr | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^[1] | |
| | 0x81 (Direct) | | | | | | | | T | |
| | PEC | | | | | | | | T | |
| Sr | DevID[6:0] | | | | | | | W=0 | A ^{1,[2]} | |
| | 0x00 | | | | | | | DISINT | T | |
| | PEC | | | | | | | | T | |

- NOTE 1 The PMIC NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
- NOTE 2 The PMIC device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The PMIC device ignores the entire packet until STOP operation or next Repeat Start operation.
- NOTE 3 Repeat Start or Repeat Start with 7'h7E.

Table 78 — DISEC CCC Byte Encoding

| Bit | Encoding | Notes |
|--------|--|---|
| DISINT | 0 = No Action 1 = Disable IBI Interrupt | It is illegal for Host to issue DISEC CCC with DISINT bit = '0'; the PMIC may ignore it or subsequent PMIC operation may not be guaranteed and the PMIC may require Bus Reset |

7.5.10.3 RSTDAA CCC

The RSTDAA CCC is only supported after device is put in I3C Basic mode. In I²C mode, this CCC is ignored (i.e., the RSTDAA command is not executed internally and any bytes arriving after the 0x06 RSTDAA Broadcast CCC are ignored for all purposes, including parity checking, until the next STOP operation or Repeat START with 7'h7E is received). When RSTDAA CCC is registered by the PMIC, it updates [Table 153, Register 0x30 \[2\] = '0'](#), [Table 155, Register 0x32 \[6\] = '0'](#), it disables PEC and IBI function ([Table 158, Register 0x34 \[7:6\] = '00'](#)) and clears parity function [Table 158, Register 0x34 \[5\] = '0'](#)) and it takes in effect at the next Start operation (i.e., after STOP operation).

Table 79 through Table 80 show an example of a single RSTDAA CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 79 — RSTDAA CCC - Broadcast[illegible]

NOTE 1The PMIC NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

Table 80 — RSTDAA CCC - Broadcast with PEC

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|------------------|-------|-------|-------|-------|-------|-------|-------|------------------|------|
| S or Sr | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^[1] | |
| | 0x06 (Broadcast) | | | | | | | | T | |
| | PEC | | | | | | | | T | P |

NOTE 1 The PMIC NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

7.5.10.4 SETAASA CCC

The SETAASA CCC is only supported when device is in I²C mode. In I²C mode, when host issues this CCC, to guarantee that this CCC is registered by the device without any error, the host shall limit the maximum speed operation for this CCC to 1 MHz. In I³C Basic mode, this CCC is ignored. When SETAASA CCC is registered by the PMIC, it updates [Table 155, Register 0x32 \[6\] = '1'](#) and it takes in effect at the next Start operation (i.e., after STOP operation). [Table 81](#) shows an example of a single SETAASA CCC.

SETAASA CCC does not support PEC function as device is in I²C mode and there is no PEC function in I²C mode.

Table 81 — SETAASA CCC - Broadcast

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|------------------|-------|-------|-------|-------|-------|-------|-------|-------|------|
| S or Sr | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A | |
| | 0x29 (Broadcast) | | | | | | | | T | P |

7.5.10.5 GETSTATUS CCC

The GETSTATUS CCC is supported in I3C Basic mode. In I²C mode, this CCC is ignored (i.e., it is not executed internally and the Repeat Start byte arriving after the 0x90 GETSTATUS CCC code is not acknowledged and host must do STOP operation. [Table 82](#) through [Table 83](#) show an example of a single GETSTATUS CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 82 — GETSTATUS CCC - Direct

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|---------------|-------|-------|--------|-------------------|-------|-------|-------|------------------|------------------------|
| S or Sr | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^[1] | |
| | 0x90 (Direct) | | | | | | | | T | |
| Sr | DevID[6:0] | | | | | | | R=1 | A | |
| | PEC_Err | 0 | 0 | 0 | 0 | 0 | 0 | 0 | T=1 | |
| | 0 | 0 | P_Err | R32[3] | Pending Interrupt | | | | T=0 | Sr ^[2] or P |

NOTE 1 The PMIC NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 Repeat Start or Repeat Start with 7'h7E.

Table 83 — GETSTATUS CCC - Direct with PEC

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|-------|---------------|-------|-------|--------|-------------------|-------|-------|-------|------------------|------------------------|
| S | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^[1] | |
| | 0x90 (Direct) | | | | | | | | T | |
| | PEC | | | | | | | | T | |
| Sr | DevID[6:0] | | | | | | | R=1 | A | |
| | PEC_Err | 0 | 0 | 0 | 0 | 0 | 0 | 0 | T=1 | |
| | 0 | 0 | P_Err | R32[3] | Pending Interrupt | | | | T=1 | |
| | PEC | | | | | | | | T=0 | Sr ^[2] or P |

NOTE 1 The PMIC NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 Repeat Start or Repeat Start with 7'h7E.

7.5.10.5 GETSTATUS CCC (cont'd)

Table 84 — GETSTATUS CCC Byte Encoding

| Bit | Encoding | Notes |
|-------------------|--|---|
| PEC_Err | 0 = No Error 1 = PEC Error Occurred | This register is cleared when Host issues clear command to Table 123, Register 0x12 [3] for PEC error |
| P_Err | 0 = No Error 1 = Protocol Error; Parity Error occurred | This register is cleared when Host issues clear command to Table 123, Register 0x12 [2] for Parity error. |
| R32[3] | See Table 155, Register 0x32 for encoding. | PMIC reflects the register status of Table 155, Register 0x32 [3] in this bit. |
| Pending Interrupt | 0000 = No Pending Interrupt or No New Global Status Event 0001 = Pending Interrupt or New Global Status Event All other encodings are reserved | This register is cleared when Host issues clear command to any appropriate device status register that causes IBI status register to get cleared. |

When the PMIC device responds to GETSTATUS CCC, after it completes the response, the PEC_Err, P_Err and Pending Interrupt Bits [3:0] do not automatically get cleared. The host must explicitly clear the appropriate status register through Clear command by writing '1' to corresponding register or by issuing Global Clear command. Once the PMIC device clears the appropriate status register, only then PEC_Err, P_err and Pending Interrupt Bits [3:0] gets cleared.

After host issues clear command, if the condition is still present, the device will again set the appropriate status register, sets the IBI status register to '1' and Pending Interrupt Bits [3:0] to '0001'.

7.5.10.6 DEVCAP CCC

The DEVCAP CCC is only supported after device is put in I3C Basic mode. In I²C mode, it is illegal for host to issue this CCC; the PMIC may ignore it or subsequent PMIC operation may not be guaranteed and the PMIC may require Bus Reset. [Table 85](#) through [Table 86](#) show an example of a single DEVCAP CCC. [Table 87](#) defines the encoding for DEVCAP CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 85 — DEVCAP CCC - Direct

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|-----------------------------------|-------|-------|-------|-------|-------|-------|-------|------------------|------------------------|
| S or Sr | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^[1] | |
| | 0xE0 (Direct) | | | | | | | | T | |
| Sr | DevID[6:0] | | | | | | | R=1 | A ¹ | |
| | MSB (Each bit defines capability) | | | | | | | | T=1 | |
| | LSB (Each bit defines capability) | | | | | | | | T=0 | Sr ^[2] or P |

NOTE 1 The PMIC NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 Repeat Start or Repeat Start with 7'h7E.

7.5.10.6 GETSTATUS CCC (cont'd)**Table 86 — DEVCAP CCC - Direct with PEC**

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|-----------------------------------|-------|-------|-------|-------|-------|-------|-------|------------------|------------------------|
| S or Sr | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^[1] | |
| | 0xE0 (Direct) | | | | | | | | T | |
| | PEC | | | | | | | | T | |
| Sr | DevID[6:0] | | | | | | | R=1 | A ¹ | |
| | MSB (Each bit defines capability) | | | | | | | | T=1 | |
| | LSB (Each bit defines capability) | | | | | | | | T=1 | |
| | PEC | | | | | | | | T=0 | |
| | | | | | | | | | | Sr ^[2] or P |

NOTE 1 The PMIC NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 Repeat Start or Repeat Start with 7'h7E.

Table 87 — DEVCAP CCC Byte Encoding

| Bit | Encoding | Notes |
|-----------|--|-----------------|
| MSB [7] | RFU | Coded as '0' |
| MSB [6] | RFU | Coded as '0' |
| MSB [5] | RFU | Coded as '0' |
| MSB [4] | RFU | Coded as '0' |
| MSB [3] | RFU | Coded as '0' |
| MSB [2] | 0 = No Support for Timer based Reset 1 = Supports Timer based Reset | Coded as '1' |
| MSB [1:0] | RFU | Coded as '00' |
| LSB [7:0] | RFU | Coded as '0x00' |

7.5.10.7 SETHID CCC

The SETHID CCC is supported only when device is in I²C mode. In I²C mode, when host issues this CCC, to guarantee that this CCC is registered by the device without any error, the host shall limit the maximum speed operation for this CCC to 1 MHz. In I³C Basic mode, it is illegal for host to issue this CCC; the PMIC may ignore it or subsequent PMIC operation may not be guaranteed and the PMIC may require Bus Reset. When SETHID CCC is registered by the PMIC, it updates [Table 158, Register 0x34 \[3:1\]](#) with the HID code received by the PMIC and it takes in effect at the next Start operation (i.e., after STOP operation). [Table 88](#) shows an example of a single SETHID CCC. As the device is in I²C mode when SETHID CCC is issued, the PEC function is not supported.

7.5.10.7 SETHID CCC (cont'd)

Once PMIC receives SETHID CCC and updates its 3-bit HID code, after the Stop operation, PMIC device only responds to updated 7-bit address. The 4-bit LID code of the PMIC device remains as is.

The Host may issue SETHID CCC more than one time.

Table 88 — SETHID CCC - Broadcast

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|------------------|-------|-------|-------|----------|-------|-------|-------|-------|------|
| S or Sr | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A | |
| | 0x61 (Broadcast) | | | | | | | | T | |
| | 0 | 0 | 0 | 0 | HID[2:0] | | | 0 | T | P |

7.5.10.8 DEVCTRL CCC

On a typical I3C Basic bus there can be up to 120 devices. For DDR5 DIMM application environment, there are up to 8 SPD5 Hub devices and behind each SPD5 Hub devices, there are 4 local target devices totaling up to 40 or more devices on I3C Basic bus. For certain operations such as enable or disable functions that are common to all devices (i.e., Packet Error Check), the host must go through one device at a time which takes significant amount of time at initial power up. Further, it requires additional complexity on the host because it must speak different protocol depending on how it may access the device until all devices are configured identically.

To help expedite this configuration operation and to simplify the host complexity, the device supports the DEVCTRL CCC. The DEVCTRL CCC is supported either in I²C mode or I3C Basic mode of operation. In I²C mode, when host issues this CCC, to guarantee that this CCC is registered by the device without any error, the host shall limit the maximum speed operation for this CCC to 1 MHz. [Table 89](#) through [Table 90](#) show an example of a single DEVCTRL CCC.

In I3C mode only, if PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

The host shall pay attention to DEVCTRL CCC. If DEVCTRL CCC is used to access device specific registers (e.g., RegMod = '1'), the host shall still follow any device specific register restriction. For example, if device specific register requires STOP operation for device to take in the effect of the setting, the host must also use STOP operation when using DEVCTRL CCC to access device specific register.

7.5.10.8 DEVCTRL CCC (cont'd)**Table 89 — DEVCTRL CCC - Broadcast**

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|---------------------|-------|-------|------------------|-------|-------------|-------|--------|------------------|------|
| S or Sr | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^[1] | |
| | 0x62 (Broadcast) | | | | | | | | T | |
| | AddrMask[2:0] | | | StartOffset[1:0] | | PEC BL[1:0] | | RegMod | T | |
| | DevID[6:0] | | | | | | | 0 | T ^[2] | |
| | Byte 0 Data Payload | | | | | | | | T | |
| | Byte 1 Data Payload | | | | | | | | T | |
| | Byte 2 Data Payload | | | | | | | | T | |
| | Byte 3 Data Payload | | | | | | | | T | |

NOTE 1 The PMIC NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 An exception is made for DEVCTRL CCC. The PMIC does not report parity error when it determines 7-bit device select code issues by the host does not match with its own device code. If 7-bit device select code does not match but if parity is still valid, the device does not check for parity error in subsequent bytes; ignores the entire packet and waits until STOP or Repeat Start operation.

NOTE 3 Repeat Start or Repeat Start with 7'h7E.

Table 90 — DEVCTRL CCC - Broadcast with PEC^[1]

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|---------|---------------------|-------|-------|------------------|-------|-------------|-------|--------|------------------|------------------------|
| S or Sr | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^[2] | |
| | 0x62 (Broadcast) | | | | | | | | T | |
| | AddrMask[2:0] | | | StartOffset[1:0] | | PEC BL[1:0] | | RegMod | T | |
| | DevID[6:0] | | | | | | | 0 | T ^[3] | |
| | Byte 0 Data Payload | | | | | | | | T | |
| | Byte 1 Data Payload | | | | | | | | T | |
| | Byte 2 Data Payload | | | | | | | | T | |
| | Byte 3 Data Payload | | | | | | | | T | |
| | PEC | | | | | | | | T | Sr ^[4] or P |

NOTE 1 DEVCTRL CCC with PEC check is only supported in I3C mode.

NOTE 2 The PMIC NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 An exception is made for DEVCTRL CCC. The PMIC does not report parity error when it determines 7-bit device select code issues by the host does not match with its own device code. The device does not check for PEC as all subsequent bytes are discarded due to parity error. If 7-bit device select code does not match but if parity is still valid, the device does not check for parity error in subsequent bytes; ignores the entire packet and waits until STOP or Repeat Start operation.

NOTE 4 Repeat Start or Repeat Start with 7'h7E.

7.5.10.8 DEVCTRL CCC (cont'd)

Table 91 — DEVCTRL CCC Command Definition

| Parameter | Definition |
|------------------|--|
| AddrMask[2:0] | <p>Broadcast, Unicast or Multicast Command Selection</p> <p>000 = Unicast Command; PMIC device responds if DevID[6:0] field matches with PMIC device's own 7-bit address (4-bit LID + 3-bit HID)</p> <p>011 = Multicast Command; PMIC device and possible other device responds if DevID[6:3] field matches with PMIC device's own 4-bit LID address</p> <p>111 = Broadcast Command; All devices respond to this command</p> <p>All other encodings are reserved</p> |
| StartOffset[1:0] | <p>Only applicable if RegMod = '0'</p> <p>Identifies the starting Byte (Byte 0 or Byte 1 or Byte 2 or Byte 3) for DEVCTRL CCC. Host can start at any Byte (from Byte 0 to Byte 3) and has continuous access to next byte until STOP operation. If Byte 3 is reached, the host is responsible for applying STOP operation.</p> <p>00 = Byte 0 01 = Byte 1 10 = Byte 2 11 = Byte 3</p> |
| PEC BL[1:0] | <p>Only applicable if RegMod = '0' and PEC function is enabled.</p> <p>Identifies the burst length just for this DEVCTRL CCC. The device uses the setting in this field to know when the PEC byte is expected after the data bytes.</p> <p>00 = 1 Byte 01 = 2 Byte 10 = 3 Byte 11 = 4 Byte</p> |
| RegMod | <p>Identifies if DEVCTRL is going to be used for General Registers as identified in Byte 0 to Byte 3 or device specific address offset register.</p> <p>0 = Access to General Registers in Byte 0 to Byte 3 (i.e., StartOffset[1:0] = Valid) 1 = Device Specific Offset Address (i.e., StartOffset[1:0] & PECBL[1:0] is a don't care and does not apply). The Host shall NOT use RegMod = '1' with Broadcast Command if there are different types of devices on the I3C Basic bus.</p> |
| DevID[6:0] | <p>Identifies 7-bit device address. Device responds to DEVCTRL CCC data packet depending on AddrMask[2:0].</p> <p>If AddrMask[2:0] = '111', DevID[6:0] is a don't care and device always responds. If AddrMask[2:0] = '000', DevID[6:0] must match for device to respond If AddrMask[2:0] = '011', DevID[6:3] must match for device to respond. DevID[2:0] is don't care. For any other codes for AddrMask[2:0], the device always NACKs.</p> |

7.5.10.8 DEVCTRL CCC (cont'd)**Table 92 — DEVCTRL CCC Data Payload Definition**

| Byte # | Bit # | Function | Definition | Comment |
|--------|-------|--------------------|---|--|
| Byte 0 | [7] | PEC Enable | 0 = Disable 1 = Enable | Table 158, Register 0x34 [7] is updated |
| | [6] | Parity Disable | 0 = Enable 1 = Disable | Table 158, Register 0x34 [5] is updated |
| | [5:2] | RFU | RFU | |
| | [1] | VR Enable | 0 = VR Disable 1 = VR Enable | Table 155, Register 0x32 [7] is updated. |
| | [0] | RFU | RFU | |
| Byte 1 | [7:4] | RFU | RFU | |
| | [3] | Global & IBI Clear | 0 = No Action 1 = Clear All Event and pending IBI ^[1] | Table 125, Register 0x14 [0] is updated. |
| | [2:0] | RFU | RFU | |
| Byte 2 | [7:0] | RFU | RFU | |
| Byte 3 | [7:0] | RFU | RFU | |

NOTE 1 After target device clears the event, the device can still have certain registers set to '1' if the event is still present, in which case, the device will generate an IBI again at the next opportunity.

7.5.10.8.1 DEVCTRL CCC Examples - RegMod = '0'

Table 93 shows an example of DEVCTRL CCC data packet. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host uses DEVCTRL CCC as Multicast command. Host sends Multicast command to all devices with 4-bit LID code of '1001' on I3C Basic bus to do VR Enable followed by all devices with 4-bit LID code of '0110' to disable parity function. The host sends AddrMask = '011' to indicate Multicast command with DevID[6:3] match; StartOffset = '00' to indicate starting Byte 0 and RegMod = '0' to indicates general register. Upon receiving this command, all devices with DevID[6:3] that matches to '1001' will do the VR Enable command and DevID[6:3] that matches to '0110' with disable the parity function.

Table 93 — DEVCTRL CCC Example - Multicast Command to '1001' and '0110' Devices

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|-------|------------------|-------|-------|-------|-------|-------|-------|-------|------------------|------|
| S | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^[1] | |
| | 0x62 (Broadcast) | | | | | | | | T | |
| | 011 | | | 00 | | 00 | | 0 | T | |
| | 1001 000 | | | | | | | 0 | T | |
| | 0000 0010 | | | | | | | | T | |
| Sr | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ¹ | |

Table 93 — DEVCTRL CCC Example - Multicast Command to '1001' and '0110' Devices (cont'd)

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|-------|------------------|-------|-------|-------|-------|-------|-------|-------|-------|------|
| | 0x62 (Broadcast) | | | | | | | | T | |
| | 011 | | | 00 | | 00 | | 0 | T | |
| | 0110 000 | | | | | | | 0 | T | |
| | 0100 0000 | | | | | | | | T | P |

NOTE 1 See Figure 22 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

Table 94 shows an example of DEVCTRL CCC data packet. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host uses DEVCTRL CCC as Broadcast command to enable PEC function. The host sends AddrMask = '111' to indicate Broadcast command; StartOffset = '00' to indicate starting Byte 0 and RegMod = '0' to indicate general register. Upon receiving this command, all devices will enable PEC function.

Table 94 — DEVCTRL CCC Example - Broadcast Command to all Devices

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|-----------|------------------|-------|-------|-------|-------|-------|-------|-------|------------------|------|
| S | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^[1] | |
| | 0x62 (Broadcast) | | | | | | | | T | |
| | 111 | | | 00 | | 00 | | 0 | T | |
| | 0000 000 | | | | | | | 0 | T | |
| 1000 0000 | | | | | | | | | T | P |

NOTE 1 See Figure 22 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

Table 95 shows an example of DEVCTRL CCC data packet. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host uses DEVCTRL CCC as Unicast command to enable VR on DIMM5. The host sends AddrMask = '000' to indicate Unicast command; StartOffset = '00' to indicate starting Byte 0 and RegMod = '0' to indicate general register. Upon receiving this command, PMIC on DIMM5 will enable its regulator.

Table 95 — DEVCTRL CCC Example - Unicast Command to PMIC on DIMM5

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|-------|------------------|-------|-------|-------|-------|-------|-------|-------|------------------|------|
| S | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^[1] | |
| | 0x62 (Broadcast) | | | | | | | | T | |
| | 000 | | | 00 | | 00 | | 0 | T | |
| | 1001 101 | | | | | | | 0 | T | |
| | 0000 0010 | | | | | | | | T | |

NOTE 1 See Figure 22 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

7.5.10.8.2 DEVCTRL CCC Examples - RegMod = '1'

Table 96 shows an example of DEVCTRL CCC data packet for the purpose of configuring device specific address offset register. It assumes that all devices on the bus are already in I3C Basic mode with PEC function enabled and parity function enabled. In this example, the Host sends Multicast command to all devices with 4-bit LID code of '0010' on the I3C Basic bus to write to address offset of 0x1C and 0x1D with data 0xFF and 0x55 respectively followed by all devices with 4-bit LID of '1001' on the I3C Basic bus to write to address offset of 0x15 with data 0x78.

The PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 96 — DEVCTRL CCC Example - Multicast Command to '0010' and '1001' Devices

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|-------|---|-------|-------|-------|-------|-------|-------|-------|------------------|------|
| S | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^[1] | |
| | 0x62 (Broadcast) | | | | | | | | T | |
| | 011 | | | 00 | | 00 | | 1 | T | |
| | 0010 000 | | | | | | | 0 | T | |
| | 0001 1100 (address offset 0x1C) | | | | | | | | T | |
| | 0010 0000 (CMD field = 2 bytes of data) | | | | | | | | T | |
| | 1111 1111 (data) | | | | | | | | T | |
| | 0101 0101 (data) | | | | | | | | T | |
| | PEC | | | | | | | | T | |
| Sr | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ¹ | |
| | 0x62 (Broadcast) | | | | | | | | T | |
| | 011 | | | 00 | | 00 | | 1 | T | |
| | 1001 000 | | | | | | | 0 | T | |
| | 0001 0101 (address offset 0x15) | | | | | | | | T | |
| | 0000 0000 (CMD field = 1 byte of data) | | | | | | | | T | |
| | 0111 1000 (data) | | | | | | | | T | |
| | PEC | | | | | | | | T | |

NOTE 1 See Figure 22 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

Table 97 shows an example of DEVCTRL CCC data packet for the purpose of configuring device specific address offset register. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host sends Multicast command to all devices with 4-bit LID code of '1001' on the I3C Basic bus to write to address offset of 0x13 with data 0xFF and it continues to write data 0x01 to the next address.

7.5.10.8.2 DEVCTRL CCC Examples - RegMod = '1' (cont'd)

Table 97 — DEVCTRL CCC Example - Multicast Command to '1001' Devices

| Start | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | A/N/T | Stop |
|-------|---------------------------------|-------|-------|-------|-------|-------|-------|-------|------------------|------|
| S | 1 | 1 | 1 | 1 | 1 | 1 | 0 | W=0 | A ^[1] | |
| | 0x62 (Broadcast) | | | | | | | | T | |
| | 011 | | | 00 | | 00 | | 1 | T | |
| | 1001 000 | | | | | | | 0 | T | |
| | 0001 0011 (address offset 0x13) | | | | | | | | T | |
| | 1111 1111 (data) | | | | | | | | T | |
| | 0000 0001 (data) | | | | | | | | T | |

NOTE 1 See Figure 22 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

7.6 IO Operation

At power on, by default, the PMIC device comes up in legacy I²C mode of operation with Open Drain IO for its interface. The maximum speed is limited to 1 MHz and supported IO voltage levels are from 1.0 V to 3.3 V.

After power on, the host may put the PMIC device in I3C Basic mode of operation.

In I3C Basic mode, the host may drive the SCL clock input of the PMIC device using either Push-Pull output driver or the open-drain output driver. It is expected that for all DDR5 DIMM family environment, the host may always drive the SCL clock input using a Push-Pull output driver.

To support in band interrupt, the PMIC device supports dynamic switching between Open Drain mode and Push Pull mode on its SDA bus for various events. Table 98 describes the different modes of operation by the PMIC device for each cycle.

Table 98 — PMIC Device Dynamic IO Operation Mode Switching

| | Open Drain Mode | Push Pull Mode |
|--|-----------------|----------------|
| START + Device Select Code | Yes | No |
| START + 7'h7E IBI Header Byte | Yes | No |
| REPEAT START + Device Select Code | No | Yes |
| REPEAT START + 7'h7E Header Byte | No | Yes |
| CCC Bytes (i.e., after 7'h7E+W=0+ACK) | No | Yes |
| STOP | No | Yes |
| ACK/NACK Responses | Yes | No |
| Command, Block Address, Address Operation | No | Yes |
| Interrupt Request by Target + Device Select Code | Yes | No |
| IBI Payload | No | Yes |
| Write Data, T-bit sequence | No | Yes |
| Read Data, T-bit sequence | No | Yes |
| PEC, T-bit sequence | No | Yes |

7.7 Bus Clear

The PMIC device supports the following described Bus Clear feature in I²C mode only. Any attempt by host to perform I²C Bus clear on a target device in I3C mode may result in an active drive bus contention on the SDA data line.

There may be abnormal circumstances when the host abruptly stops clocking SCL while the target device is in the middle of outputting data for read operation. For these types of events, the SDA data line may appear as stuck low as the device is expecting to receive more clock pulses from the host. Eventually when the host has control of the SCL clock, the host may optionally clear the device that is stuck low on the SDA data line by sending continuous 18 clock pulses without driving the SDA data line followed by STOP operation. The device floats the SDA line within 18 clock pulses and returns to the Idle state. The device is ready for normal new transactions with Start condition.

7.8 Bus Reset

To prevent a malfunctioning device from locking up the I²C bus or I3C Basic bus, a bus reset mechanism is defined. It uses a timeout mechanism on SCL as shown in [Figure 29](#) to force a device bus reset. All devices on a I²C or I3C Basic bus reset simultaneously. Bus reset operation works same way regardless of whether device is operating in I²C or I3C Basic mode.

To guarantee the device resets I²C bus or I3C Basic bus, the SCL clock input Low time has to be greater than or equal to $t_{\text{TIMEOUT(Max)}}$.

The PMIC device does not reset I²C bus or I3C Basic bus if the SCL clock input Low time is less than $t_{\text{TIMEOUT(Min)}}$.

If the SCL clock input Low time is between $t_{\text{TIMEOUT(Min)}}$ and $t_{\text{TIMEOUT(Max)}}$, the PMIC device does not guarantee and it may or may not reset the I²C bus or I3C Basic bus.

When RESET, the PMIC device takes following actions.

1. Interface and any pending command or transactions are cleared
2. All internal register values are preserved unless noted otherwise in item # 3 below.
3. Device returns to I²C mode of operation; resets [Table 115, Register 0x0A \[3:2\]](#) to '00', [Table 153, Register 0x30 \[2\]](#) to '0', [Table 155, Register 0x32 \[6\]](#) to '0', [Table 158, Register 0x34 \[7:5\]](#) resets to '000', [Table 158, Register 0x34 \[3:1\]](#) resets to '111'.
4. Device does not re-sample PID pin.
5. Device floats the SDA pin such that it gets pulled High by external/other device pullup.
6. Device treats bus reset as STOP operation.

7.8 Bus Reset (cont'd)

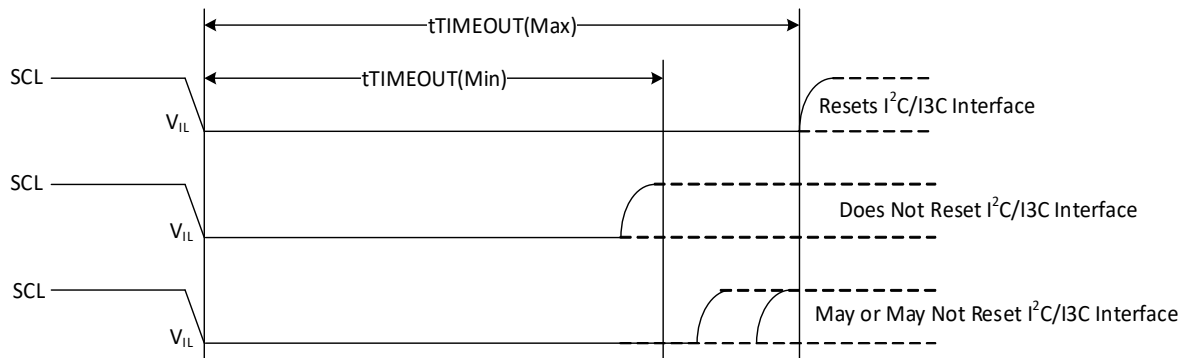


Figure 29 — I²C or I³C Basic Bus Reset - PMIC Device

7.9 Command Truth Table

The command truth table as shown in Table 99 only applies in I³C Basic mode with PEC enabled for the CMD field (bits [7:5] for Write and Read data packet). In I²C mode and I³C Basic mode with PEC disabled, the command truth table does not apply.

Table 99 — For I³C Mode only with PEC Enabled - Command Truth Table

| TS5 Command | Command Name | CMD Code | RW | Address |
|----------------------------|--------------|---------------------|------------------|---------------------|
| | | 2nd Byte Bits [7:5] | 2nd Byte Bit [4] | 1st Byte Bits [7:0] |
| Write 1 Byte to Register | W1R | 000 | 0 | V |
| Read 1 Byte from Register | R1R | | 1 | V |
| Write 2 Byte to Register | W2R | 001 | 0 | V |
| Read 2 Byte from Register | R2R | | 1 | V |
| Write 4 Byte to Register | W4R | 010 | 0 | V |
| Read 4 Byte from Register | R4R | | 1 | V |
| Write 16 Byte to Register | W16R | 011 | 0 | V |
| Read 16 Byte from Register | R16R | | 1 | V |
| Reserved | RSVD | 100 to 111 | RSVD | RSVD |

8 Example Schematic

Figure 30 shows an example schematic when PMIC is configured in one three phase regulator, one dual phase regulator and one single phase regulator mode configuration. Table 100 shows all component details shown in the schematics. Note that distributed capacitance across the entire DIMM module is not shown in the schematic.

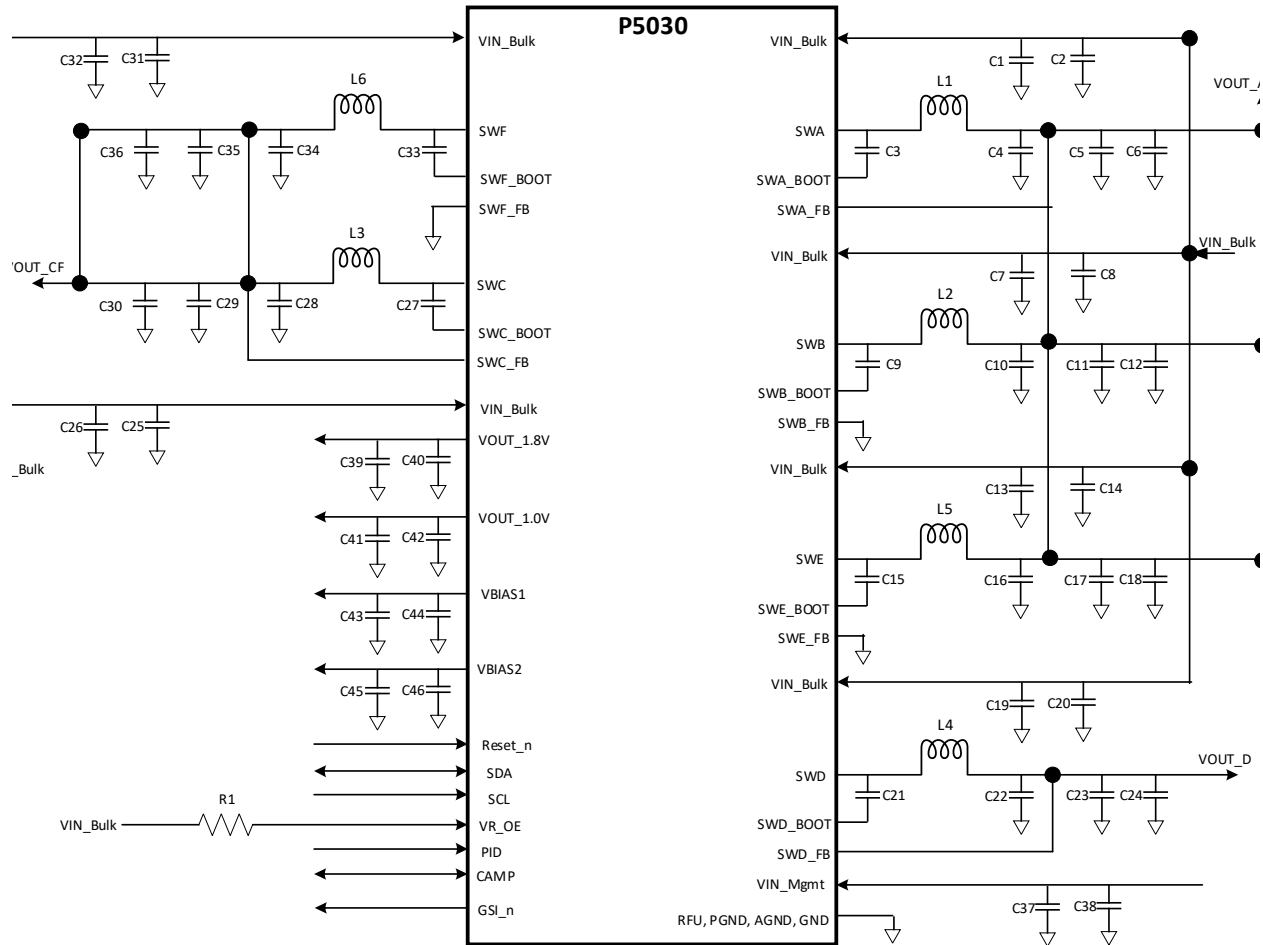


Figure 30 — Three Phase+ Dual Phase + Single Phase (3-2-1) Regulator Example Schematic

8 Example Schematic (cont'd)

Table 100 — PMIC Schematic Values

| Remark | Component | Quantity | Value | Physical Size | Unit | Comment |
|-----------|------------------------|----------|-------|--------------------------|------|---------|
| SWA | L1 | 1 | 0.47 | 4.3 mm x 4.3 mm x 2.0 mm | μH | |
| SWB | L2 | 1 | 0.47 | 4.3 mm x 4.3 mm x 2.0 mm | μH | |
| SWE | L3 | 1 | 0.47 | 4.3 mm x 4.3 mm x 2.0 mm | μH | |
| SWC | L4 | 1 | 0.47 | 4.3 mm x 4.3 mm x 2.0 mm | μH | |
| SWF | L5 | 1 | 0.47 | 4.3 mm x 4.3 mm x 2.0 mm | μH | |
| SWD | L6 | 1 | 1.0 | 4.3 mm x 4.3 mm x 2.0 mm | μH | |
| SWA | C1 | 1 | 0.1 | 0201; 25V | μF | |
| | C2 ^[1] | 2 | 22 | 0805; 25V | μF | 2x22 |
| | C3 | 1 | 0.1 | 0201; 25V | μF | |
| | C4 | 1 | 47 | 0603; 6.3V | μF | |
| | C5 | 1 | 47 | 0603; 6.3V | μF | |
| | C6 ^[1] | 2 | 47 | 0603; 6.3V | μF | 2x47 |
| SWB | C7 | 1 | 0.1 | 0201; 25V | μF | |
| | C8 ^[1] | 2 | 22 | 0805; 25V | μF | 2x22 |
| | C9 | 1 | 0.1 | 0201; 25V | μF | |
| | C10 | 1 | 47 | 0603; 6.3V | μF | |
| | C11 | 1 | 47 | 0603; 6.3V | μF | |
| | C12 ^[1] | 2 | 47 | 0603; 6.3V | μF | 2x47 |
| SWE | C13 | 1 | 0.1 | 0201; 25V | μF | |
| | C14 ^[1] | 2 | 22 | 0805; 25V | μF | 2x22 |
| | C15 | 1 | 0.1 | 0201; 25V | μF | |
| | C16 | 1 | 47 | 0603; 6.3V | μF | |
| | C17 | 1 | 47 | 0603; 6.3V | μF | |
| | C18 ^{[1],[2]} | 2 | 47 | 0603; 6.3V | μF | 2x47 |
| SWC | C25 | 1 | 0.1 | 0201; 25V | μF | |
| | C26 ^[1] | 2 | 22 | 0805; 25V | μF | 2x22 |
| | C27 | 1 | 0.1 | 0201; 25V | μF | |
| | C28 | 1 | 47 | 0603; 6.3V | μF | |
| | C29 | 1 | 47 | 0603; 6.3V | μF | |
| | C30 ^[1] | 2 | 47 | 0603; 6.3V | μF | 2x47 |
| SWF | C31 | 1 | 0.1 | 0201; 25V | μF | |
| | C32 ^[1] | 2 | 22 | 0805; 25V | μF | 2x22 |
| | C33 | 1 | 0.1 | 0201; 25V | μF | |
| | C34 | 1 | 47 | 0603; 6.3V | μF | |
| | C35 | 1 | 47 | 0603; 6.3V | μF | |
| | C36 ^[1] | 2 | 47 | 0603; 6.3V | μF | 2x47 |
| SWD | C19 | 1 | 0.1 | 0201; 25V | μF | |
| | C20 ^[1] | 2 | 22 | 0805; 25V | μF | 2x22 |
| | C21 | 1 | 0.1 | 0201; 25V | μF | |
| | C22 | 1 | 47 | 0603; 6.3V | μF | |
| | C23 | 1 | 47 | 0603; 6.3V | μF | |
| | C24 | 1 | 47 | 0603; 6.3V | μF | |
| VIN_Mgmt | C37 | 1 | 0.1 | 0201; 6.3V | μF | |
| | C38 | 1 | 4.7 | 0402; 6.3V | μF | |
| VOUT_1.8V | C39 | 1 | 0.1 | 0201; 6.3V | μF | |
| | C40 | 1 | 4.7 | 0402; 6.3V | μF | |
| VOUT_1.0V | C41 | 1 | 0.1 | 0201; 6.3V | μF | |
| | C42 | 1 | 4.7 | 0402; 6.3V | μF | |
| VBIAS1 | C43 | 1 | 0.1 | 0201; 6.3V | μF | |
| | C44 | 1 | 4.7 | 0402; 6.3V | μF | |
| VBIAS2 | C45 | 1 | 0.1 | 0201; 6.3V | μF | |
| | C46 | 1 | 4.7 | 0402; 6.3V | μF | |
| VR_OE | R1 | 1 | 200 | 0201 | KΩ | |

NOTE 1 This represents physically two different capacitors. Each with value as shown in "Value" column.

NOTE 2 For three phase DIMM design, due to component placement limitation of bulk output capacitance for SWE, some of the bulk output capacitance can be substituted with distributed capacitance to overcome the physical limitation of the PCB.

8 Example Schematic (cont'd)

Figure 31 shows an example schematic when PMIC is configured as two dual phase regulators and one single phase regulator mode configuration. Table 100 shows all component details shown in the schematics. Note that distributed capacitance across the entire DIMM module is not shown in the schematic.

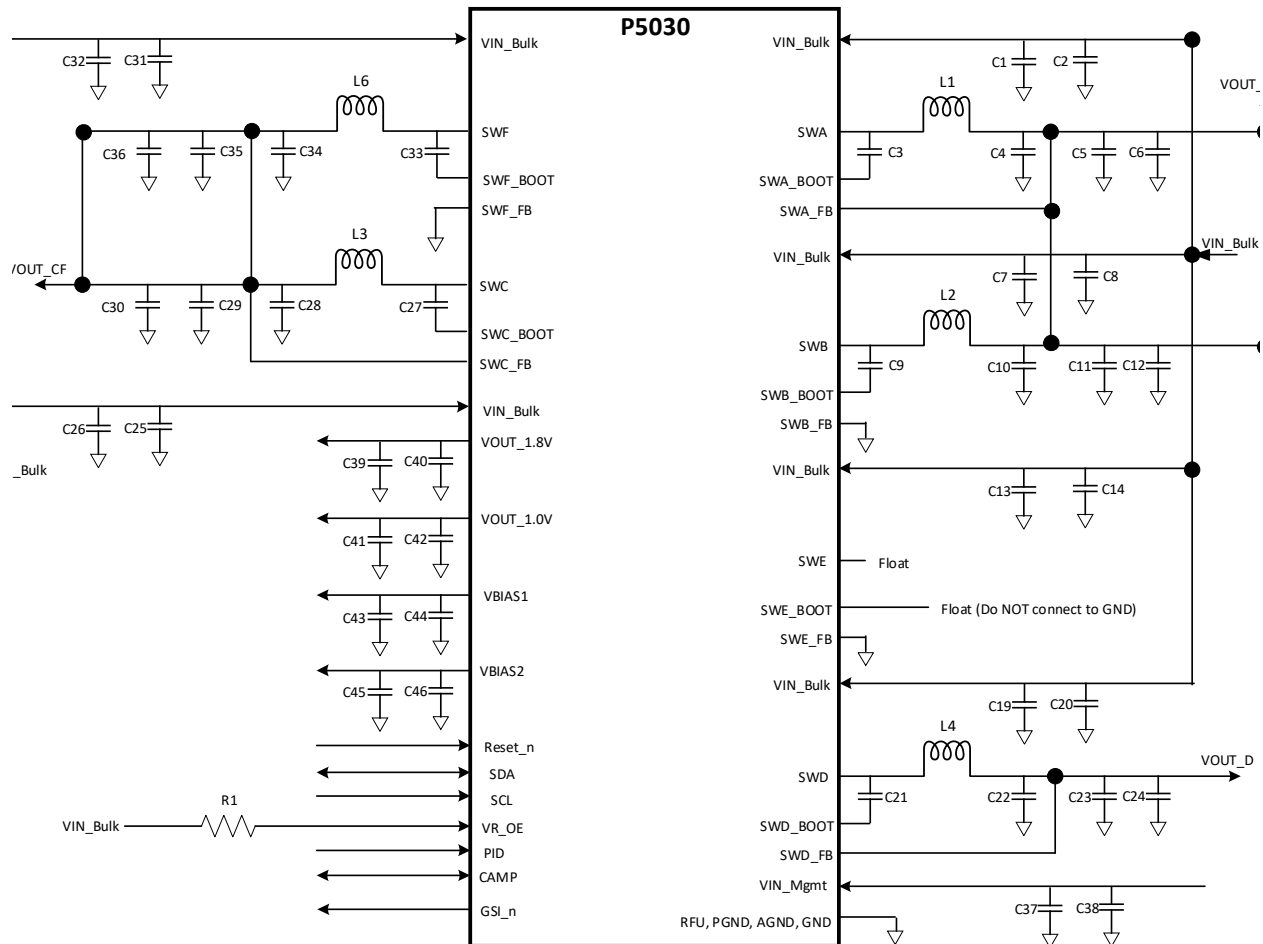


Figure 31 — Dual Phase + Dual Phase + Single Phase (2-2-1) Regulator Example Schematic

8 Example Schematic (cont'd)

Figure 32 shows an example schematic when PMIC is configured as one dual phase regulator and two single phase regulators mode configuration. Table 100 shows all component details shown in the schematics. Note that distributed capacitance across the entire DIMM module is not shown in the schematic.

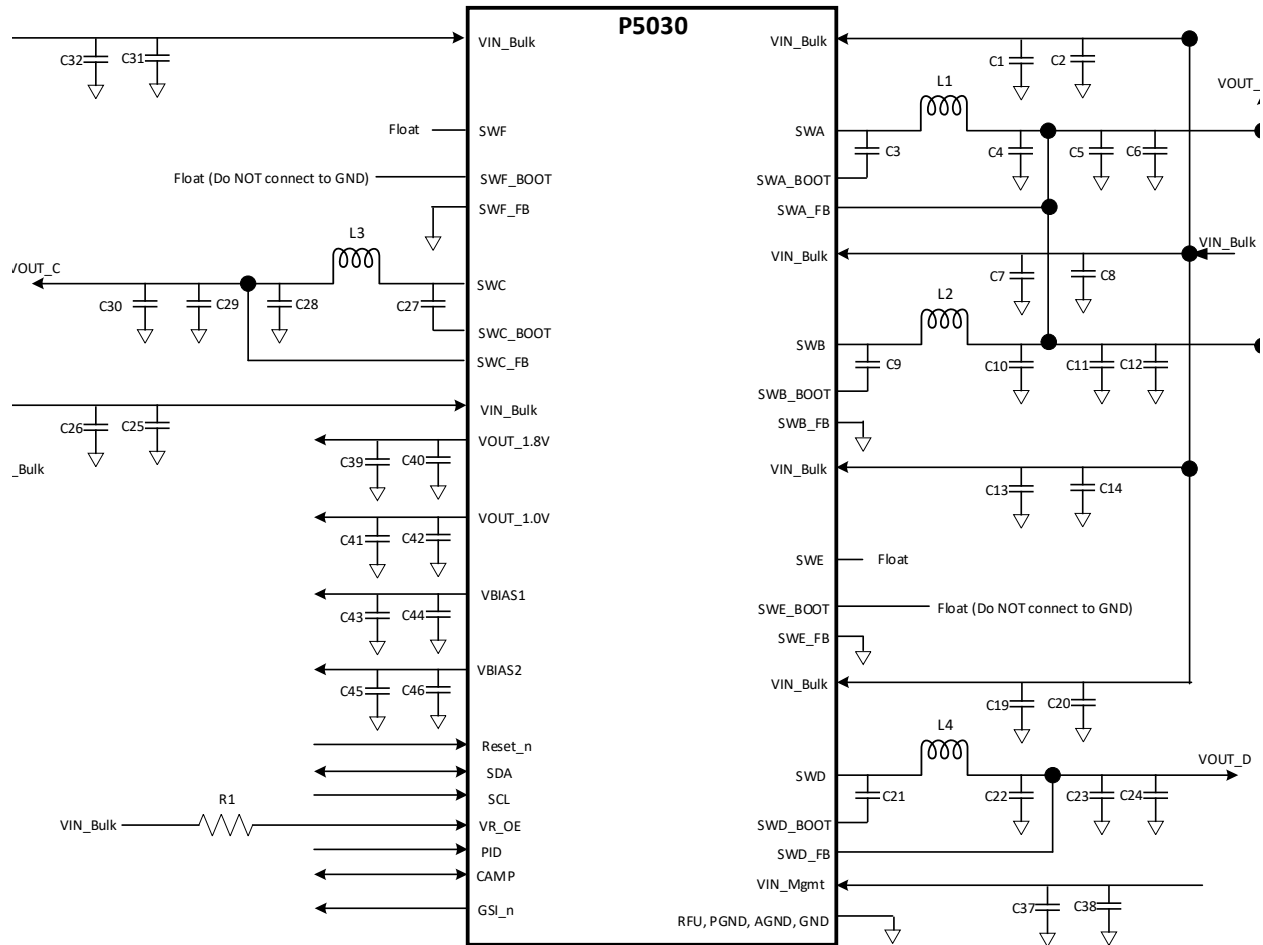


Figure 32 — Dual Phase + Single Phase + Single Phase (2-1-1) Regulator Example Schematic

8 Example Schematic (cont'd)

Figure 33 shows an example schematic when PMIC is configured as four single phase regulators configuration. Table 100 shows all component details shown in the schematics. Note that distributed capacitance across the entire DIMM module is not shown in the schematic.

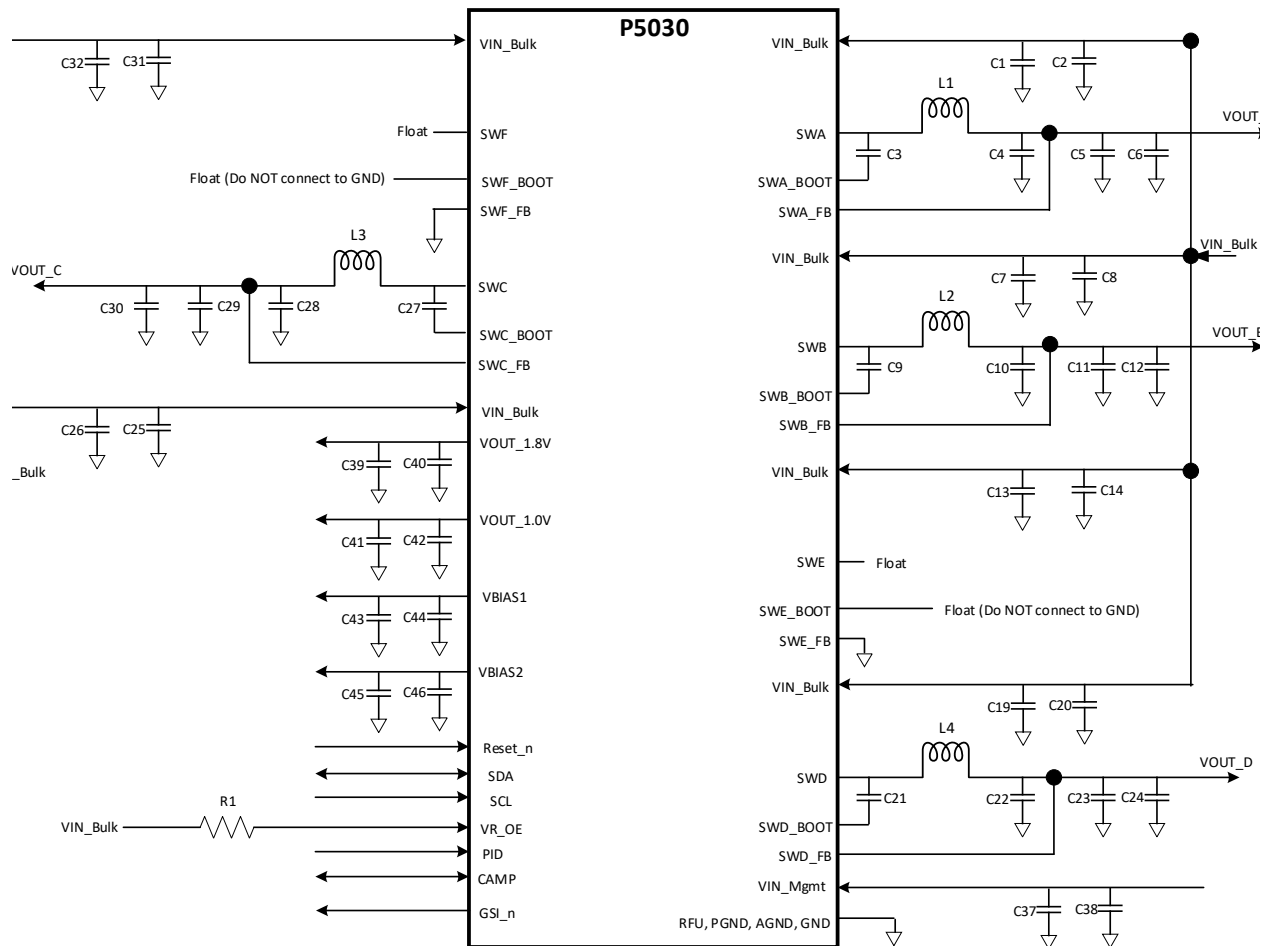


Figure 33 — Single Phase + Single Phase + Single Phase + Single Phase (1-1-1-1) Regulator Example Schematic

9 Inductor Specification

9.1 Mechanical Specification

The inductor package dimensions and its recommended land patterns are defined in [Table 101](#).

Table 101 — Inductor Mechanical Specification

| Package Size | | Reference Drawing | Recommended Land Pattern |
|--------------|---------|-----------------------------|------------------------------|
| L (mm) | 4.3 Max | Figure 34 (Left Picture) | Figure 34 (Right Picture) |
| W (mm) | 4.3 Max | | |
| H (mm) | 2.0 Max | | |

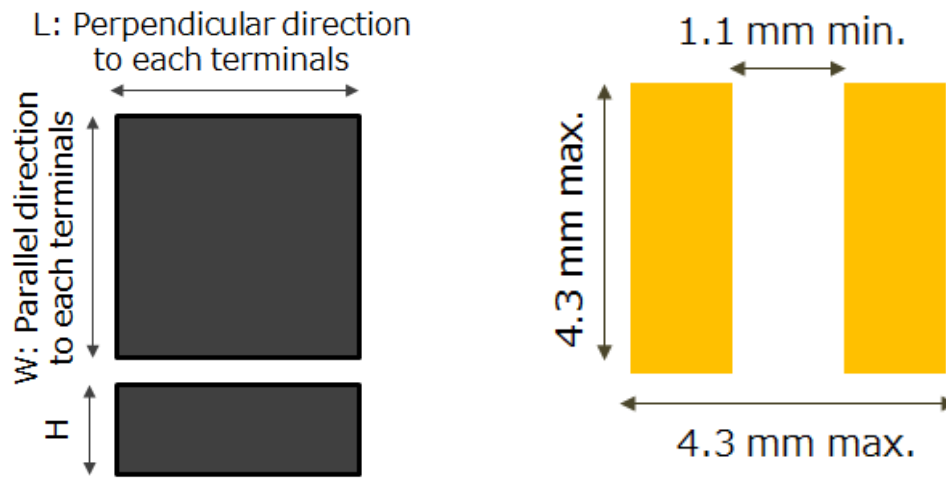


Figure 34 — Reference Drawing and Recommended Land Pattern

9.2 Electrical Specification

The inductor electrical specifications are defined in [Table 102](#).

Table 102 — Inductor Electrical Specification^[1]

| Switch Rail Target | L @ 0.5-1 MHz; 0 Bias ± 20% (μH) | Max DCR (mΩ) | Max ACR @ 1 MHz ^{[2],[3]} (mΩ) | Ipeakmax ^[4] (A) | Min L @ (Ipeakmax (μH) | Max L @ Ipeakmax (μH) |
|----------------------------|---|-----------------|---|--------------------------------|------------------------------|-----------------------------|
| SWA, SWB, SWC, SWE, SWF | 0.47 | 4.2 | 120 | 9.5 | 0.21 | 0.47 |
| SWD | 1.0 | 8.9 | 250 | 6.0 | 0.45 | 1.0 |

NOTE 1 Test condition: Ambient Temperature = 20 ± 2 °C; Ambient Humidity = $65 \pm 5\%$ Rh

NOTE 2 ACR definition: $ACR = R_s @ 1 \text{ MHz} - DCR$. Measured current (1 MHz/sinusoidal): 0.52 A rms for 0.47 μH, 0.25 A rms for 1.0 μH; with no DC Bias for all cases.

NOTE 3 For R_s measurement, it is recommended to measure by Iwatsu SY-8218 (BH Analyzer, with NF IE-1125B), its upper compatible instruments or other instruments which is guaranteed on the measurement accuracy by inductor vendors.

NOTE 4 Minimum and maximum inductance is defined at DC bias current given by definition in Ipeakmax of PMIC5030.

10 Application Notes

10.1 Identify and Map Out DIMM with a PMIC Fault in a Shared CAMP Topology

Typical DDR5 server platform may have up to 32 DDR5 DIMM sockets. Server platform implementation may vary however it is possible to have up to 8 DDR5 DIMMs may share CAMP signal. The exact number of DDR5 DIMMs that share CAMP signal is beyond the scope of this application note. It is assumed that CAMP signal is pulled up on the platform or on the controller via 1K Ohm pullup resistor to either 3.3 V or 1.8 V.

In a DDR5 server platform, it is possible that one or more DDR5 DIMM may have encountered a PMIC fault, as listed below, that has generated VR Disable event. Also refer to [Table 27](#).

- SWx Over Voltage
- SWx Under Voltage
- VIN_Bulk Over Voltage
- VIN_Bulk Under Voltage
- Critical Temperature

In this environment, it is desired to let the platform continue to power up and that faulty PMIC does not interfere with the platform operation. This application note describes a BIOS or appropriate software method to identify the faulty PMIC/DDR5 DIMM and then to map out the faulty PMIC/DDR5 DIMM from the memory subsystem. The fault scenario noted here is one example of fault scenario. Note that initial failure may occur during operation, hence BIOS needs to determine and log fault condition and then execute the map out routine.

Faulty PMIC Identification:

1. Power up the platform (i.e., DDR5 DIMMs) by applying VIN_Bulk and VIN_Mgmt input supplies.
2. Broadcast VR Enable command to all PMICs.
3. If all PMICs power up their regulators successfully, all PMICs float the CAMP signal and the pullup resistor pulls the CAMP signal high indicating that all PMICs (i.e., DDR5 DIMMs) have powered up successfully.
4. However, if one or more PMIC fails to power up their regulators then that PMIC continues to hold the CAMP signal low while other PMICs that do power up their regulators successfully floats the CAMP signal. The net effect is CAMP signal remains low.
5. BIOS eventually times out as the CAMP signal is not pulled up high and interrogates all PMIC's status registers one at a time. The interrogation process of PMIC status registers allows BIOS to identify which PMICs regulators are successfully powered up and which PMICs are faulty.

Once BIOS identifies faulty PMIC, BIOS stores the faulty PMIC (DDR5 DIMM) identification in its non-volatile memory Isolating and Securing Faulted PMIC:

10.1 Identify and Map Out DIMM with a PMIC Fault in a Shared CAMP Topology (cont'd)

1. Once the faulty PMIC is identified, the platform may re-cycle the power by simultaneously removing VIN_Bulk and VIN_Mgmt input supplies and then re-applying VIN_Bulk and VIN_Mgmt input supplies. This puts PMIC in configuration mode,
 - a. The BIOS reads PMIC error log registers to determine 'bad' PMIC. The BIOS also has a prior knowledge of a faulty PMIC.
2. BIOS performs following steps to the faulty PMIC.
 - a. Write R32 = 0x08 (Floats CAMP signal; prevents PMIC interference by writing R32[5] = '0')
 - b. Ensure R2F[2] = '0'.
3. Broadcast VR Enable command to all PMICs.
4. All good PMIC executes Power On Sequence and floats the CAMP signal. The faulty PMIC is already floating the CAMP signal and does not execute Power On Sequence.
5. At this point, BIOS sees CAMP signal is pulled High and moves to the next operation.
6. By the above process, the faulty PMIC is mapped out of the memory system in a secure state and it does not interfere with platform operation. The good PMICs allow server system to power up normally and operate in a secure state.

10.2 Error Injection Test Methodology

The PMIC error injection feature can be used many ways to test the PMIC at either component level or at the module level or at the system level. The error injection feature can be used to debug the PMIC component itself or to simulate the DIMM module behavior in a standalone ATE environment or in the system environment or to develop/simulate the system software to ensure PMIC and DIMM component hardware and system software works in a harmonious way if there is an actual fault event in the system.

The combination matrix to test each type of error injection is very large and it is the responsibility of the PMIC provider to ensure that all combinations are tested. The PMIC component specification does not provide the list in entirety but rather provides one possible general test method for error injection feature.

At all times, the PMIC specification must be followed. The test methodology does not alter or change the meaning of the PMIC specification. The test methodology may add, remove or modify steps in any sequence as long as the PMIC component specification is followed. The test results will vary depending on the starting condition and the sequence of steps. It is the responsibility of PMIC component provider to ensure results are checked against the specific condition and sequence while following the PMIC component specification.

One example of Error injection test after VR Enable command:

1. Power cycle the PMIC; Issue R39 = 0x74 command; observe CAMP and GSI_n signal.
2. Read the PMIC registers R04 to R0B, R33, R108 to R10A (checks all memory and status registers are cleared).
3. Issue the VR Enable command; read the PMIC registers R04 to R0B and R33 (check PMIC successfully turned on the rails without any fault); observe CAMP and GSI_n signal.
4. Inject error via R35, R12F and select desired error type.
5. Check PMIC regulators are turned off; read the PMIC registers R04 to R0B, R33, R108 to R10A (Check appropriate error log and status registers are set); observe CAMP and GSI_n signal.
6. Power cycle the PMIC.
7. Read the PMIC registers R04 to R07 (checks all memory).
8. Issue R39 = 0x74 command.
9. Read the PMIC registers R04 to R0B, R33, R108 to R10A.
10. Repeat another error injection test starting step # 3.

11 Registers

11.1 Register Attribute Definition

All volatile registers have Base Attributes as defined in [Table 103](#). Some register attributes are further modified with Attribute Modifiers, as defined in [Table 104](#).

Table 103 — Register Base Attributes

| Attribute | Abbreviation | Description |
|------------|--------------|---|
| Read Only | RO | This bit can be read by software. Writes have no effect. |
| Read/Write | RW | This bit can be read or written by host. |
| Write Only | W | This bit can only be written by host. Read from this bit returns '0'. |
| Reserved | RV | This bit is reserved for future expansion and its value must not be modified by host. The bit will return '0' when read. Write has no effect. |

Table 104 — Register Attribute Modifier

| Attribute | Abbreviation | Description |
|----------------|--------------|---|
| Write '1' Only | 1O | This bit can only be set (i.e., write '1') but not reset (i.e., write '0'). Write '0' has no effect. |
| Protected | P | This bit is protected by the password registers. This bit cannot be written to unless the password code has been written into the password registers. |
| Persistent | E | This bit is persistent during power cycle but Erasable with Command |
| Persistent | N | This bit is persistent during power cycle but not Erasable with Command |
| Persistent | A | This bit is read only persistent register set by the PMIC vendor during manufacturing. |

11.2 Register Map Breakdown

Table 105 — Register Map Breakdown

| Register Range | Region | Comments |
|----------------|------------------------|---|
| 0x00 - 0x3F | Host Region | Host Accessible Registers |
| 0x40 - 0x6F | DIMM Vendor Region | DIMM Vendor Registers - Non Volatile Memory Allows DIMM vendors to program the PMIC for a given DRAM/DIMM vendor designs. These are password protected registers and password is selected by DIMM vendor. Under normal operation, these registers are not used by any host. These registers require password for read access. Access to these registers without correct password will return all data as '0'. These registers require complete power cycle before it takes in effect. Changing these registers under normal operation is considered an illegal operation. |
| 0x70 - 0xFF | Vendor Specific Region | Vendor Specific Registers - Non Volatile Memory These are vendor specific password protected registers. Under normal operation these registers are not used by any host. These registers require password for read access. Access to these registers without correct password returns all data as '0'. |
| 0x100 - 0x15D | Host Region | Host Accessible Registers |

11.2.1 Register Memory Protection

The PMIC DIMM vendors registers (0x40 - 0x6F) are password protected registers. Both Read and Write access to DIMM vendor registers are blocked unless it is unlocked by providing the correct password. The default password for DIMM vendor registers is 0x9473. The PMIC offers DIMM vendors to select their own password for DIMM vendor registers.

11.2.2 Steps to Access DIMM Vendor Region Registers

The steps to access the DIMM vendor registers are as follows:

1. Write to register [Table 160, Register 0x37](#) = 8 bit password LSB code.
2. Write to register [Table 161, Register 0x38](#) = 8 bit password MSB code.
3. Write to register [Table 162, Register 0x39](#) = 0x40.
4. Perform Read operations to DIMM vendor registers as desired.
5. Write to register [Table 162, Register 0x39](#) = 0x00.

11.2.3 Steps to Change DIMM Vendor Region Password

By default, the DIMM vendor region register password is 0x9473. The steps to change the password from default password are as follows:

1. Write to register [Table 160, Register 0x37](#) = 0x73.
2. Write to register [Table 161, Register 0x38](#) = 0x94.
3. Write to register [Table 162, Register 0x39](#) = 0x40.
4. Write to register [Table 160, Register 0x37](#) = New 8 bit password LSB code as desired by DIMM vendor.
5. Write to register [Table 161, Register 0x38](#) = New 8 bit password MSB code as desired by DIMM vendor.
6. Write to register [Table 162, Register 0x39](#) = 0x80.
7. Wait 200 ms.
8. Write to register [Table 162, Register 0x39](#) = 0x00.
9. Power cycle the PMIC. (Remove VIN_Bulk and VIN_Mgmt supply from the PMIC. The new password is in effect after the power cycle.

To change the password again from this point on, repeat steps 1 to 8 but note that in steps 1 and 2 current password is required.

11.2.4 Steps to Burn or Program DIMM Vendor Region Registers

The steps to burn or to program the DIMM vendor registers are as follows:

1. Write to register [Table 160, Register 0x37](#) = 8 bit password LSB code.
2. Write to register [Table 161, Register 0x38](#) = 8 bit password MSB code.
3. Write to register [Table 162, Register 0x39](#) = 0x40.
4. Programming DIMM vendor registers are done at block level. Block 40 addresses: 0x40 - 0x4F; Block 50 addresses: 0x50 - 0x5F; Block 60 addresses: 0x60 - 0x6F. Perform write operation to each block as desired.
5. Burn each block one at a time: Block 40 addresses: Write register [Table 162, Register 0x39](#) = 0x81. Block 50 addresses: Write register [Table 162, Register 0x39](#) = 0x82. Block 60 addresses: Write register [Table 162, Register 0x39](#) = 0x85.
6. Wait time 200 ms.
7. To check if programming is complete: Perform read from register [Table 162, Register 0x39](#). The code 0x5A indicates it is complete. It takes 200 ms per block to program.
8. To verify if programming is done correctly: Perform read operation from appropriate block addresses.
9. Write to register [Table 162, Register 0x39](#) = 0x00.

11.3 Host Region Register Map

Table 106 — Register Color Coding Scheme

| Region | Register Range | Restriction |
|---|--|--|
| Host Region + DIMM Vendor Region + Vendor specific Region | Table 126, Register 0x15 to Table 152, Register 0x2F Table 155, Register 0x32 [7,5:0], Table 159, Register 0x35, Table 180, Register 0x114 to Table 181, Register 0x115, Table 182, Register 0x11A to Table 191, Register 0x123, Table 192, Register 0x12E to Table 193, Register 0x12F Table 232, Register 0x40 to Table 277, Register 0x0F Register 0x70 to Register 0xFF | Register Modification is NOT allowed in write- protect mode |
| Host Region | Table 133, Register 0x1C to Table 150, Register 0x2D Table 152, Register 0x2F [2] Table 182, Register 0x11A to Table 190, Register 0x122 | Registers are copied from DIMM Vendor Region Setting at power on |

Table 107 — Host Region - Register Map

| Register | Attribute | Description |
|--------------------------|-----------|---|
| 0x00 to 0x02 | RV | R00 [7:0] to R02 [7:0] - Reserved |
| Table 108, Register 0x03 | RON | R03 [7:4] DIMM Vendor Region MTP CRC Error Count R03 [3:0] PMIC Vendor Region MTP Error Count |
| Table 109, Register 0x04 | ROE | R04 [7] Global Error Count R04 [6:4] Global Error History Log: Buck OV/UV, VIN_Bulk OV, Critical Temperature |
| | RON | R04 [3:0] Global Error Count Enhancement |
| Table 110, Register 0x05 | ROE | R05 [7] Reserved R05 [6:3] Power On Reset - SWA, SWB, SWC & SWD Power Not Good R05 [2:0] Power On Reset - High Level Status Code |
| Table 111, Register 0x06 | ROE | R06 [7:4] Power On Reset - SWA, SWB, SWC & SWD Under Voltage Lockout R06 [3:0] Power On Reset - SWA, SWB, SWC & SWD Over Voltage |
| Table 112, Register 0x07 | ROE | R07 [7:6] Power On Reset - SWE, SWF Under Voltage Lockout R07 [5:4] Power On Reset - SWE, SWF Over Voltage R07 [3:2] Reserved R07 [1:0] Power On Reset - SWE, SWF Power Not Good |
| Table 113, Register 0x08 | RO | R08 [7] VIN_Bulk Input Power Good Status R08 [6] Critical Temperature Shutdown Status R08 [5:2] SWA, SWB, SWC, SWD Output Power Good Status R08 [1] VIN_Mgmt Input Over Voltage Status R08 [0] VIN_Bulk Input Over Voltage Status |

Table 107 — Host Region - Register Map (cont'd)

| Register | Attribute | Description |
|--|-----------|--|
| Table 114, Register 0x09 | RO | R09 [7] PMIC High Temperature Warning Status R09 [6] VBias Power Good Status R09 [5] VOUT_1.8V Output Power Good Status R09 [4] VIN_Mgmt to VIN_Bulk Input Supply Switchover Status R09 [3:0] SWA, SWB, SWC & SWD High Output Current Consumption Warning Status |
| Table 115, Register 0x0A | RO | R0A [7:4] SWA, SWB, SWC, SWD Output Over Voltage Status R0A [3] PEC Error Status R0A [2] Parity Error Status R0A [1] IBI Status R0A [0] Reserved |
| Table 116, Register 0x0B | RO | R0B [7:4] SWA, SWB, SWC & SWD Output Current Limiter Warning Status R0B [3:0] SWA, SWB, SWC & SWD Output Under Voltage Lockout Status |
| Table 117, Register 0x0C | RO | R0C [7:0] SWA Output Current or Power Measurement or Total Output Power Measurement |
| Table 118, Register 0x0D | RO | R0D [7:0] SWB Output Current or Power Measurement |
| Table 119, Register 0x0E | RO | R0E [7:0] SWC Output Current or Power Measurement |
| Table 120, Register 0x0F | RO | R0F [7:0] SWD Output Current or Power Measurement |
| Table 121, Register 0x10 | 1O | R10 [7] Clear VIN_Bulk Input Power Good Status R10 [6] Reserved R10 [5:2] Clear SWA, SWB, SWC & SWD Output Power Good Status R10 [1] Clear VIN_Mgmt Input Over Voltage Status R10 [0] Clear VIN_Bulk Input Over Voltage Status |
| Table 122, Register 0x11 | 1O | R11 [7] Clear PMIC High Temperature Warning Status R11 [6] Clear VBias Power Good Status R11 [5] Clear VOUT_1.8V Output Power Good Status R11 [4] Clear VIN_Mgmt to VIN_Bulk Input Supply Switchover Status R11 [3:0] Clear SWA, SWB, SWC & SWD High Output Current Consumption Warning Status |
| Table 123, Register 0x12 | 1O | R12 [7:4] Clear SWA, SWB, SWC, SWD Output Over Voltage Status R12 [3] Clear PEC Error R12 [2] Clear Parity Error R12 [1:0] Reserved |
| Table 124, Register 0x13 | 1O | R13 [7:4] Clear SWA, SWB, SWC & SWD Output Current Limiter Warning Status R13 [3:0] Clear SWA, SWB, SWC & SWD Output Under Voltage Lockout Status |
| Table 125, Register 0x14 | 1O | R14 [7:5] Reserved R14 [4] Clear VIN_Mgmt Power Good Status in Switchover Mode R14 [3] Clear VBias Output or VIN_Bulk Input Under Voltage Lockout Status R14 [2] Clear VOUT_1.0V Output Power Good Status R14 [1] Reserved R14 [0] Clear Global Status |

Table 107 — Host Region - Register Map (cont'd)

| Register | Attribute | Description |
|--------------------------|-----------|---|
| Table 126, Register 0x15 | RW | R15 [7] Mask VIN_Bulk Input Power Good Status R15 [6] Reserved R15 [5:2] Mask SWA, SWB, SWC & SWD Output Power Good Status R15 [1] Mask VIN_Mgmt Input Over Voltage Status R15 [0] Mask VIN_Bulk Input Over Voltage Status |
| Table 127, Register 0x16 | RW | R16 [7] Mask PMIC High Temperature Warning Status R16 [6] Mask VBIAS Power Good Status R16 [5] Mask VOUT_1.8V Output Power Good Status R16 [4] Mask VIN_Mgmt to VIN_Bulk Input Supply Switchover Status R16 [3:0] Mask SWA, SWB, SWC & SWD High Output Current Consumption Warning Status |
| Table 128, Register 0x17 | RW | R17 [7:4] Mask SWA, SWB, SWC, SWD Output Over Voltage Status R17 [3] Mask PEC Error Status R17 [2] Mask Parity Error Status R17 [1:0] Reserved |
| Table 129, Register 0x18 | RW | R18 [7:4] Mask SWA, SWB, SWC & SWD Output Current Limiter Warning Status R18 [3:0] Mask SWA, SWB, SWC & SWD Output Under Voltage Lockout Status |
| Table 130, Register 0x19 | RW | R19 [7:5] Reserved R19 [4] Mask VIN_Mgmt Power Good Status Switchover Mode Status R19 [3] Mask Vbias Output or VIN_Bulk Input Under Voltage Lockout Status R19 [2] Mask VOUT_1.0V Output Power Good Status R19 [1:0] Reserved |
| Table 131, Register 0x1A | RW | R1A [7:5] VIN_Bulk Input Power Good Threshold Voltage R1A [4] Reserved R1A [3] VBIAS Power Good Threshold Voltage R1A [2] VOUT_1.8 V Power Good Threshold Voltage R1A [1] Output Power Measurement Select R1A [0] VOUT_1.0 V Power Good Threshold Voltage |
| Table 132, Register 0x1B | RW | R1B [7] VIN_Bulk Input Over Voltage Threshold R1B [6] Current or Power Meter Select R1B [5] VIN_Mgmt Input Over Voltage Threshold R1B [4] Global Mask Control for PWR_GOOD Output Pin R1B [3] GSI_n Pin Enable R1B [2:0] PMIC High Temperature Warning Threshold |
| Table 133, Register 0x1C | RW | R1C [7:0] SWA Output High Current Consumption Warning Threshold |
| Table 134, Register 0x1D | RW | R1D [7:0] SWB Output High Current Consumption Warning Threshold |
| Table 135, Register 0x1E | RW | R1E [7:0] SWC Output High Current Consumption Warning Threshold |
| Table 136, Register 0x1F | RW | R1F [7:0] SWD Output High Current Consumption Warning Threshold |
| Table 137, Register 0x20 | RW | R20 [7:6] SWA Output Current Limiter Warning Threshold R20 [5:4] SWB Output Current Limiter Warning Threshold R20 [3:2] SWC Output Current Limiter Warning Threshold R20 [1:0] SWD Output Current Limiter Warning Threshold |

Table 107 — Host Region - Register Map (cont'd)

| Register | Attribute | Description |
|--------------------------|-----------|---|
| Table 138, Register 0x21 | RW | R21 [7:1] SWA Voltage Setting R21 [0] SWA Power Good Low Side Threshold |
| Table 139, Register 0x22 | RW | R22 [7:6] SWA Power Good High Side Threshold R22 [5:4] SWA Over Voltage Threshold R22 [3:2] SWA Under Voltage Lockout Threshold R22 [1:0] SWA Soft Stop Time |
| Table 140, Register 0x23 | RW | R23 [7:1] SWB Voltage Setting R23 [0] SWB Power Good Low Side Threshold |
| Table 141, Register 0x24 | RW | R24 [7:6] SWB Power Good High Side Threshold R24 [5:4] SWB Over Voltage Threshold R24 [3:2] SWB Under Voltage Lockout Threshold R24 [1:0] SWB Soft Stop Time |
| Table 142, Register 0x25 | RW | R25 [7:1] SWC Voltage Setting R25 [0] SWC Power Good Low Side Threshold |
| Table 143, Register 0x26 | RW | R26 [7:6] SWC Power Good High Side Threshold R26 [5:4] SWC Over Voltage Threshold R26 [3:2] SWC Under Voltage Lockout Threshold R26 [1:0] SWC Soft Stop Time |
| Table 144, Register 0x27 | RW | R27 [7:1] SWD Voltage Setting R27 [0] SWD Power Good Low Side Threshold |
| Table 145, Register 0x28 | RW | R28 [7:6] SWD Power Good High Side Threshold R28 [5:4] SWD Over Voltage Threshold R28 [3:2] SWD Under Voltage Lockout Threshold R28 [1:0] SWD Soft Stop Time |
| Table 146, Register 0x29 | RW | R29 [7:6] SWA Mode Select R29 [5:4] SWA Switching Frequency R29 [3:2] SWB Mode Select R29 [1:0] SWB Switching Frequency |
| Table 147, Register 0x2A | RW | R2A [7:6] SWC Mode Select R2A [5:4] SWC Switching Frequency R2A [3:2] SWD Mode Select R2A [1:0] SWD Switching Frequency |
| Table 148, Register 0x2B | RW | R2B [7:6] VOUT_1.8V LDO Setting R2B [5:3] Output Voltage Range Selection for SWA, SWB and SWC R2B [2:1] VOUT_1.0V LDO Setting R2B [0] Output Voltage Range Selection for SWD |
| Table 149, Register 0x2C | RW | R2C [7:5] SWA Soft Start Time R2C [4] Reserved R2C [3:1] SWB Soft Start Time R2C [0] Reserved |

Table 107 — Host Region - Register Map (cont'd)

| Register | Attribute | Description |
|--------------------------|-----------|---|
| Table 150, Register 0x2D | RW | R2D [7:5] SWC Soft Start Time R2D [4] Reserved R2D [3:1] SWD Soft Start Time R2D [0] Reserved |
| Table 151, Register 0x2E | RW | R2E [7:3] Reserved R2E [2:0] PMIC Shutdown temperature threshold |
| Table 152, Register 0x2F | RW | R2F [7] VIN_Mgmt Input Supply Switchover Threshold Voltage R2F [6:3] SWA, SWB, SWC & SWD Enable |
| | RW | R2F [2] Write-protect Function Control |
| | RW | R2F [1:0] Mask Bits Register Control |
| Table 153, Register 0x30 | RW | R30 [7] ADC Enable R30 [6:3] ADC Select R30 [2] Register Addressing Mode R30 [1:0] ADC Register Update Frequency |
| Table 154, Register 0x31 | RO | R31 [7:0] ADC Read Out |
| Table 155, Register 0x32 | RW, RO | R32 [7] VR Enable R32 [6] Management Interface Selection R32 [5] Execute VR Enable Control R32 [4] Execute CAMP Fail_n Function Control R32 [3] CAMP Power Good Output Signal Control R32 [2] Reserved R32 [1:0] ADC Accuracy Step Size |
| Table 157, Register 0x33 | RO | R33 [7:5] Temperature Measurement R33 [4] VIN_Mgmt Power Good Status in Switchover Mode Only R33 [3] VBIAS Output or VIN_Bulk Input Under Voltage Lockout Status R33 [2] VOUT_1.0V Output Power Good Status R33 [1:0] Reserved |
| Table 158, Register 0x34 | RV, RO | R34 [7] PEC Enable R34 [6] IBI Enable R34 [5] Parity Disable R34 [4] Reserved R34 [3:1] HID_CODE R34 [0] Reserved |
| Table 159, Register 0x35 | RW | R35 [7] Error Injection Enable R35 [6:4] Input, Output Rail Selection R35 [3] Over and Under Voltage Selection R35 [2:0] Misc. Error Injection Type |
| 0x36 | RV | R36 [7:0] Reserved |
| Table 160, Register 0x37 | WO | R37 [7:0] Password Lower Byte 0 |
| Table 161, Register 0x38 | WO | R38 [7:0] Password Upper Byte 1 |
| Table 162, Register 0x39 | RW | R39 [7:0] Command Codes |

Table 107 — Host Region - Register Map (cont'd)

| Register | Attribute | Description |
|---|-----------|--|
| Table 163, Register 0x3A | RW, 1O | R3A [7] Reserved R3A [6] Default Read Address Pointer Enable R3A [5:4] Default Read Address Pointer Selection R3A [3:2] Burst Length for Default Read Address Pointer Mode in PEC Enabled Mode R3A [1] Bypass DIMM Vendor Region CRC Error R3A [0] Check DIMM Vendor Region CRC |
| Table 164, Register 0x3B | ROA | R3B [7:6] PMIC Current Capability Extension R3B [5:4] Major Revision ID R3B [3:1] Minor Revision ID R3B [0] PMIC Current Capability |
| Table 165, Register 0x3C | ROA | R3C [7:0] VENDOR_ID_BYTE0 |
| Table 166, Register 0x3D | ROA | R3D [7:0] VENDOR_ID_BYTE1 |
| 0x3E to 0x3F | RV | R3E [7:0] to R3F [7:0] Reserved |
| Table 167, Register 0x100 | RO | R100 [7:6] SWA Output Current or Power Measurement MSB R100 [5:4] SWB Output Current or Power Measurement MSB R100 [3:2] SWC Output Current or Power Measurement MSB R100 [1:0] SWD Output Current or Power Measurement MSB |
| Table 168, Register 0x101 | RO, RV | R101 [7:6] SWE Output Current or Power Measurement MSB R101 [5:4] SWF Output Current or Power Measurement MSB R101 [3] Reserved R101 [2:0] Total Power Measurement MSB |
| Table 169, Register 0x102 | RO | R102 [7:0] SWA Output Current or Power Measurement or Total Power Measurement LSB |
| Table 170, Register 0x103 | RO | R103 [7:0] SWB Output Current or Power Measurement LSB |
| Table 171, Register 0x104 | RO | R104 [7:0] SWC Output Current or Power Measurement LSB |
| Table 172, Register 0x105 | RO | R105 [7:0] SWD Output Current or Power Measurement LSB |
| Table 173, Register 0x106 | RO | R106 [7:0] SWE Output Current or Power Measurement LSB |
| Table 174, Register 0x107 | RO | R107 [7:0] SWF Output Current or Power Measurement LSB |
| Table 175, Register 0x108 | RO | R108 [7:6] SWE, SWF Output Power Good Status R108 [5:4] SWE, SWF High Output Current Consumption Warning Status R108 [3:2] SWE, SWF Output Over Voltage Status R108 [1:0] SWE, SWF Output Current Limiter Warning Status |
| Table 176, Register 0x109 | RO, RV | R109 [7:6] SWE, SWF Output Under Voltage Lockout Status R109 [5:1] Reserved R109 [0] DIMM Region CRC Error Status from Command |
| Table 177, Register 0x10A | RO, RV | R10A [7] DIMM Vendor Region MTP CRC Error Check Status R10A [6] DIMM Vendor Region MTP CRC Error Status R10A [5] PMIC Vendor Region MTP Error Check Status R10A [4] PMIC Vendor Region MTP Error Status R10A [3:0] Reserved |
| 0x10B to 0x10D | RV | R10B [7:0] to R10D [7:0] Reserved |

Table 107 — Host Region - Register Map (cont'd)

| Register | Attribute | Description |
|---------------------------|-----------|---|
| Table 178, Register 0x10E | 1O | R10E [7:6] Clear SWE, SWF Output Power Good Status R10E [5:4] Clear SWE, SWF High Output Current Consumption Warning Status R10E [3:2] Clear SWE, SWF Output Over Voltage Status R10E [1:0] Clear SWE, SWF Output Current Limiter Warning Status |
| Table 179, Register 0x10F | 1O, RV | R10F [7:6] Clear SWE, SWF Output Under Voltage Lockout Status R10F [5:1] Reserved R10F [0] Clear DIMM Region CRC Error Status from Command |
| 0x110 to 0x113 | RV | R110 [7:0] to R113 [7:0] Reserved |
| Table 180, Register 0x114 | RW | R114 [7:6] Mask SWE, SWF Output Power Good Status R114 [5:4] Mask SWE, SWF High Output Current Consumption Warning Status R114 [3:2] Mask SWE, SWF Output Over Voltage Status R114 [1:0] Mask SWE, SWF Output Current Limiter Warning Status |
| Table 181, Register 0x115 | RW, RV | R115 [7:6] Mask SWE, SWF Output Under Voltage Lockout Status R115 [5:0] Reserved |
| 0x116 to 0x119 | RV | R116 [7:0] to R119 [7:0] Reserved |
| Table 182, Register 0x11A | RW | R11A [7:0] SWE Output High Current Consumption Warning Threshold |
| Table 183, Register 0x11B | RW | R11B [7:0] SWF Output High Current Consumption Warning Threshold |
| Table 184, Register 0x11C | RW | R11C [7:6] SWE Output Current Limiter Warning Threshold R11C [5:4] SWF Output Current Limiter Warning Threshold R11C [3:1] Output Voltage Range selection for SWE, SWF R11C [0] Output Voltage Range selection SWC Extension |
| Table 185, Register 0x11D | RW | R11D [7:1] SWE Voltage Setting R11D [0] SWE Power Good Low Side Threshold |
| Table 186, Register 0x11E | RW | R11E [7:6] SWE Power Good High Side Threshold R11E [5:4] SWE Over Voltage Threshold R11E [3:2] SWE Under Voltage Lockout Threshold R11E [1:0] SWE Soft Stop Time |
| Table 187, Register 0x11F | RW | R11F [7:1] SWF Voltage Setting R11F [0] SWF Power Good Low Side Threshold |
| Table 188, Register 0x120 | RW | R120 [7:6] SWF Power Good High Side Threshold R120 [5:4] SWF Over Voltage Threshold R120 [3:2] SWF Under Voltage Lockout Threshold R120 [1:0] SWF Soft Stop Time |
| Table 189, Register 0x121 | RW | R121 [7:6] SWE Mode Select R121 [5:4] SWE Switching Frequency R121 [3:2] SWF Mode Select R121 [1:0] SWF Switching Frequency |
| Table 190, Register 0x122 | RW, RV | R122 [7:5] SWE Soft Start Time R122 [4] Reserved R122 [3:1] SWF Soft Start Time R122 [0] Reserved |

Table 107 — Host Region - Register Map (cont'd)

| Register | Attribute | Description |
|--|-----------|--|
| Table 191, Register 0x123 | RV, RW | R123 [7:2] Reserved R123 [1:0] SWE, SWF Enable |
| 0x124 to 0x12D | RV | Reserved |
| Table 192, Register 0x12E | RW, RV | R12E [7:6] Reset_n Control R12E [5:0] Reserved |
| Table 193, Register 0x12F | RW, RV | R12F [7:6] Reserved R12F [5:4] Error Injection - Output Rail Selection R12F [3:2] Reserved R12F [1:0] Error Injection - MTP Selection |
| Table 194, Register 0x130 | ROA | R130 [7:0] Serial Number Byte 0 |
| Table 195, Register 0x131 | ROA | R131 [7:0] Serial Number Byte 1 |
| Table 196, Register 0x132 | ROA | R132 [7:0] Serial Number Byte 2 |
| Table 197, Register 0x133 | ROA | R133 [7:0] Serial Number Byte 3 |
| Table 198, Register 0x134 | ROA | R134 [7:0] Serial Number Byte 4 |
| Table 199, Register 0x135 | ROA | R135 [7:0] Serial Number Byte 5 |
| Table 200, Register 0x136 | ROA | R136 [7:0] Serial Number Byte 6 |
| 0x137 to 0x13F | RV | Reserved |
| Table 201, Register 0x140 Table 202, Register 0x141 | RON | 1st Fault Error Log |
| Table 203, Register 0x142 Table 204, Register 0x143 | RON | 2nd Fault Error Log |
| Table 205, Register 0x144 Table 206, Register 0x145 | RON | 3rd Fault Error Log |
| Table 207, Register 0x146 Table 208, Register 0x147 | RON | 4th Fault Error Log |
| Table 209, Register 0x148 Table 210, Register 0x149 | RON | 5th Fault Error Log |
| Table 211, Register 0x14A Table 212, Register 0x14B | RON | 6th Fault Error Log |
| Table 213, Register 0x14C Table 214, Register 0x14D | RON | 7th Fault Error Log |
| Table 215, Register 0x14E Table 216, Register 0x14F | RON | 8th Fault Error Log |
| Table 217, Register 0x150 Table 218, Register 0x151 | RON | 9th Fault Error Log |
| Table 219, Register 0x152 Table 220, Register 0x153 | RON | 10th Fault Error Log |
| Table 221, Register 0x154 Table 222, Register 0x155 | RON | 11th Fault Error Log |

Table 107 — Host Region - Register Map (cont'd)

| Register | Attribute | Description |
|--|-----------|----------------------|
| Table 223, Register 0x156 Table 224, Register 0x157 | RON | 12th Fault Error Log |
| Table 225, Register 0x158 Table 226, Register 0x159 | RON | 13th Fault Error Log |
| Table 227, Register 0x15A Table 228, Register 0x15B | RON | 14th Fault Error Log |
| Table 229, Register 0x15C Table 230, Register 0x15D | RON | 15th Fault Error Log |

11.4 Host Region Register Definition

11.4.1 Status Registers

The PMIC offers status registers that are grouped into four different categories.

1. Global History of Error Log Register (Table 108, Register 0x03 [7:0], Table 109, Register 0x04 [7:0])
2. Error Log Registers (Table 110, Register 0x05 [6:0], Table 111, Register 0x06 [7:0], Table 112, Register 0x07 [7:4, 1:0]).
3. Real time Status Registers (Table 113, Register 0x08 [7:0], Table 114, Register 0x09 [7:0], Table 115, Register 0x0A [7:1], Table 116, Register 0x0B [7:0], Table 157, Register 0x33 [4:2], Table 175, Register 0x108 [7:0], Table 176, Register 0x109 [7:6, 0], Table 177, Register 0x10A [7:4])
4. Periodic Status Registers (Table 117, Register 0x0C [7:0] to Table 120, Register 0x0F [7:0], Table 157, Register 0x33 [7:5], Table 167, Register 0x100 [7:0], Table 168, Register 0x101 [7:4, 2:0], Table 169, Register 0x102 [7:0] to Table 174, Register 0x107 [7:0])

Global History of Error Log Registers (Table 108, Register 0x03 [7:0])

- This register reports the cumulative error of MTP NVM check at each power on for DIMM vendor region and PMIC vendor region MTP. The PMIC writes the register bits [7:4] on its own when it detects mismatch in CRC code for DIMM vendor region and the register bits [3:0] when it detects an error for PMIC vendor region.
- The register bits Table 108, Register 0x03 [7:0] are not erasable by any command by the host and shall be preserved by the PMIC. See clause 6.30 for additional details.

Global History of Error Log Registers (Table 109, Register 0x04 [7:0])

- This register records the PMIC state at each abnormal power down cycle. This register reports the cumulative error of each abnormal power down sequence. The PMIC writes this register on its own when it internally generates VR Disable command on its own due to failure.
- The host can erase the register bits Table 109, Register 0x04 [7:4] in MTP memory and clear the status register by writing the code 0x74 in Table 162, Register 0x39. The register bits Table 109, Register 0x04 [3:0] are not erasable by any command by the host and shall be preserved by the PMIC. See clause 6.29 for additional details.

11.4.1 Status Registers (cont'd)

Error Log Registers (Table 110, Register 0x05 [6:0], Table 111, Register 0x06 [7:0] to Table 112, Register 0x07 [7:4,1:0])

- These registers record the PMIC state at each power down sequence. The PMIC may report abnormal power down sequence or normal power down sequence. The PMIC writes these registers and updates MTP when it internally generates a VR Disable command on its own due to failure. At next power up, the registers are restored from MTP to be read by the host and MTP is cleared by the PMIC. A value of '0' in the register indicates no fault event occurred prior to last power down cycle.
- The host can clear the status registers and associated MTP by writing the code 0x74 in Table 162, Register 0x39. See Figure 35 for illustration. The top waveform illustrates how PMIC captures Error Log Registers (R05 to R07) when there is a fault and how PMIC reports error log registers when PMIC goes through power down cycle. The bottom waveform illustrates same as top waveform with one exception. It shows no fault condition when CAMP is asserted to turn off switch regulator outputs with power down sequence.
- The word Power Cycle is used interchangeably with Power Down Cycle as illustrated in both figures and it means both VIN_Bulk and VIN_Mgmt input supplies are removed and re-applied. Power Down Sequence means execution of Power Off Sequence configuration registers (Table 256, Register 0x58 to Table 260, Register 0x5C, Table 266, Register 0x62, Table 269, Register 0x65, and Table 270, Register 0x66).

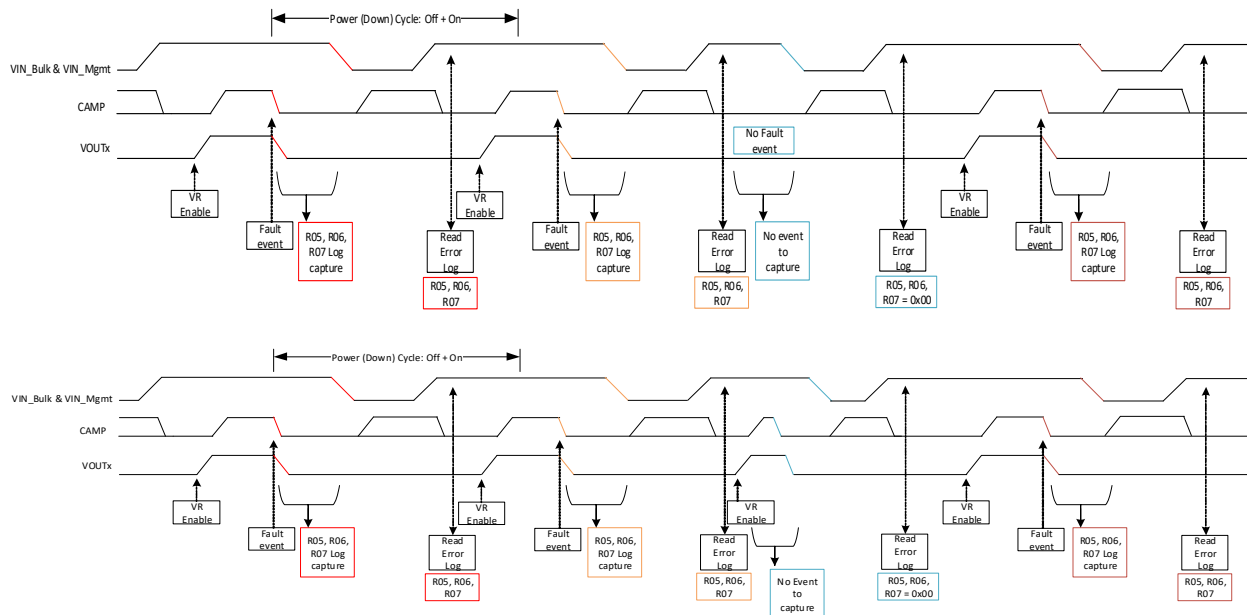


Figure 35 — Error Log (R05 to R07) Registers Behavior with Power Cycle

11.4.1 Status Registers (cont'd)

Real Time Status Registers ([Table 113, Register 0x08 \[7:0\]](#), [Table 114, Register 0x09 \[7:0\]](#), [Table 115, Register 0x0A \[7:1\]](#), to [Table 116, Register 0x0B \[7:0\]](#), [Table 157, Register 0x33 \[4:2\]](#), [Table 175, Register 0x108 \[7:0\]](#), [Table 176, Register 0x109 \[7:6, 0\]](#), [Table 177, Register 0x10A \[7:4\]](#))

- These registers are one time latched registers. Once the PMIC sets the register flag to '1' based on the event that occurs, the host must explicitly clear the register appropriately. The PMIC does not automatically update the register on its own and the status registers remains at '1' even if the event that triggered the status is no longer present. An exception is applied to [Table 177, Register 0x10A \[7:4\]](#) as it cannot be cleared by the host.
- Any switch regulator related status registers are only applicable after VR Enable command is registered by the PMIC. The PMIC updates switch regulators related status registers after VR Enable command is registered within tPMIC_PWR_GOOD_OUT time if there is any issue and host shall check these status registers after tPMIC_PWR_GOOD_OUT time. The PMIC updates these status registers if there is any event related to switch regulators in future. The GSI_n interrupt or PWR_GOOD interrupt may be generated by the PMIC at the same time depending on the type of event. The interrupts are only generated if they are not masked.
- The status registers [Table 113, Register 0x08 \[7\]](#) is only valid once valid VIN_Bulk input supply is reached at the PMIC input pin.
- The status registers [Table 114, Register 0x09 \[5\]](#), [Table 115, Register 0x0A \[3:1\]](#) and [Table 157, Register 0x33 \[2\]](#) are only valid once valid VIN_Mgmt input supply is reached at the PMIC input pin at first power on. These registers are also valid when PMIC switches over to VIN_Bulk input supply.
- The remaining status registers are valid after VR Enable command is registered.

Periodic Status Registers ([Table 117, Register 0x0C \[7:0\]](#) to [Table 120, Register 0x0F \[7:0\]](#), [Table 157, Register 0x33 \[7:5\]](#), [Table 167, Register 0x100 \[7:0\]](#), [Table 168, Register 0x101 \[7:4, 2:0\]](#), [Table 169, Register 0x102 \[7:0\]](#) to [Table 174, Register 0x107 \[7:0\]](#))

- These registers are updated periodically at certain frequency and they represent the status at that point. All these registers except for [Table 157, Register 0x33 \[7:5\]](#) are only valid after VR Enable command is registered by the PMIC.
- The register [Table 157, Register 0x33 \[7:5\]](#) is valid before and after VR Enable command.

11.4.1 Status Registers (cont'd)

Table 108 — Register 0x03

| R03 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description ^[1] |
| 7:4 | RON | 0 | R03 [7:4]: DIMM_VENDOR_REGION_MTP_ERROR_COUNT DIMM Vendor Region MTP Error Count ^[2] 0000 = 0 Error 0001 = 1 Error 0010 = 2 Errors ... 1111 = ≥ 15 Errors |
| 3:0 | RON | 0 | R04 [3:0]: PMIC_VENDOR_REGION_MTP_ERROR_COUNT PMIC Vendor Region MTP Error Count ^[2] 0000 = 0 Error 0001 = 1 Error 0010 = 2 Errors ... 1111 = ≥ 15 Errors |

NOTE 1 The PMIC shall attempt to write this register into its non-volatile memory. However, it may not be guaranteed depending on how fast the host may shut off the input power to the PMIC. The PMIC needs minimum of 4.0 V for VIN_Bulk voltage and 200 ms duration from CAMP signal assertion to guarantee the write operation into non-volatile memory.

NOTE 2 See Clause 6.30 for additional details.

11.4.1 Status Registers (cont'd)

Table 109 — Register 0x04

| R04 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description ^{[1],[2],[3]} |
| 7 | ROE | 0 | R04 [7]: GLOBAL_ERROR_COUNT Global Error Count Since Last Erase Operation ^[4] 0 = No Error or Only 1 Error since last Erase operation 1 = > 1 Error Count since last Erase operation |
| 6 | ROE | 0 | R04 [6]: GLOBAL_ERROR_LOG_BUCK_OV_OR_UV Global Error Log History for Buck Regulator Output Over or Under Voltage 0 = No Error Occurred 1 = Error Occurred |
| 5 | ROE | 0 | R04 [5]: GLOBAL_ERROR_LOG_VIN_BULK_OVER_VOLTAGE Global Error Log History for VIN_Bulk Over Voltage 0 = No Error Occurred 1 = Error Occurred |
| 4 | ROE | 0 | R04 [4]: GLOBAL_ERROR_LOG_CRITICAL_TEMPERATURE Global Error Log History for Critical Temperature 0 = No Error Occurred 1 = Error Occurred |
| 3:0 | RON | 0 | R04 [3:0]: GLOBAL_ERROR_COUNT_EN Global Error Count ^[5] 0000 = 0 Fault 0001 = 1 Error (See R140/R141 for detailed error log) 0010 = 2 Errors (See R142/R143 for detailed error log) 0010 = 3 Errors (See R144/145 for detailed error log) ... 1111 = 15 Errors (See R15C/R15D for detailed error log) Errors beyond 15 are not captured. |

NOTE 1 The PMIC shall attempt to write this register into its non-volatile memory. However, it may not be guaranteed depending on how fast the host may shut off the input power to the PMIC. The PMIC needs minimum of 4.0 V for VIN_Bulk voltage and 200 ms duration from CAMP signal assertion to guarantee the write operation into non-volatile memory.

NOTE 2 Host must explicitly perform Erase operation to erase the register [Table 109, Register 0x04 \[7:4\]](#) via [Table 162, Register 0x39](#) command. The PMIC needs minimum of 200 ms for Erase operation. Note that [Table 109, Register 0x04 \[3:0\]](#) are not erasable by the command.

NOTE 3 The error log registers are only updated when there is a VR Disable fault when the buck regulators are under regulation. For any external command registered by the PMIC from the host (i.e., VR Disable command or CAMP assertion), followed by VIN_Bulk input supply removal to the PMIC, the PMIC does not log the error log registers.

NOTE 4 PMIC counts the error since last erase operation and if more than one error occurs, it sets this bit to '1'.

NOTE 5 See clause [6.29](#) for additional details.

11.4.1 Status Registers (cont'd)

Table 110 — Register 0x05

| R05 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^{[1],[2],[3]} |
| 7 | RV | 0 | R05 [7]: Reserved |
| 6 | ROE | 0 | R05 [6]: SWA_POWER_GOOD PMIC Power On - SWA Power Not Good ^[4] 0 = Normal Power On 1 = SWA Power Not Good |
| 5 | ROE | 0 | R05 [5]: SWB_POWER_GOOD PMIC Power On - SWB Power Not Good ^{[3],[5]} 0 = Normal Power On 1 = SWB Power Not Good |
| 4 | ROE | 0 | R05 [4]: SWC_POWER_GOOD PMIC Power On - SWC Power Not Good ^[3] 0 = Normal Power On 1 = SWC Power Not Good |
| 3 | ROE | 0 | R05 [3]: SWD_POWER_GOOD PMIC Power On - SWD Power Not Good ^[3] 0 = Normal Power On 1 = SWD Power Not Good |
| 2:0 | ROE | 0 | R05 [2:0]: PMIC_ERROR_LOG PMIC Power On - High Level Status Bit to Previous Last Known Power Cycle 000 = Normal Power On 001 = Reserved 010 = Buck Regulator Output Over or Under Voltage ^[6] 011 = Critical Temperature 100 = VIN_Bulk Input Over Voltage 101 = Reserved 110 = Reserved 111 = VIN_Bulk_UV_OR_VBIAS_UV |

NOTE 1 The PMIC shall attempt to write this register into its non-volatile memory. However, it may not be guaranteed depending on how fast the host may shut off the input power to the PMIC. The PMIC needs minimum of 4.0V for VIN_Bulk voltage and 200 ms duration from CAMP signal assertion to guarantee the write operation into non-volatile memory.

NOTE 2 This entire register status reflects previous power down cycle of the PMIC and is updated by the PMIC on its own at each power cycle, if update is needed. Because this register is updated only if there is an update needed, there is no NVM life time impact. This register is cleared when host issues the erase command via [Table 162, Register 0x39](#). The PMIC needs minimum of 200 ms for Erase operation.

NOTE 3 The error log registers are only updated when there is a VR Disable fault when the buck regulators are under regulation. For any external command registered by the PMIC from the host (i.e., VR Disable command or CAMP assertion), followed by VIN_Bulk input supply removal to the PMIC, the PMIC does not log the error log registers.

NOTE 4 This register is set only if PMIC generates internal VR Disable command due to fault condition.

NOTE 5 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 6 This code is a logical OR function of [Table 111, Register 0x06](#) [7:0] and [Table 112, Register 0x07](#) [7:4] register bits.

11.4.1 Status Registers (cont'd)

Table 111 — Register 0x06

| R06 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^{[1],[2],[3]} |
| 7 | ROE | 0 | R06 [7]: SWA_UNDER_VOLTAGE_LOCKOUT PMIC Power On - SWA Under Voltage Lockout 0 = Normal Power On 1 = SWA Under Voltage Lockout |
| 6 | ROE | 0 | R06 [6]: SWB_UNDER_VOLTAGE_LOCKOUT PMIC Power On - SWB Under Voltage Lockout ^[4] 0 = Normal Power On 1 = SWB Under Voltage Lockout |
| 5 | ROE | 0 | R06 [5]: SWC_UNDER_VOLTAGE_LOCKOUT PMIC Power On - SWC Under Voltage Lockout 0 = Normal Power On 1 = SWC Under Voltage Lockout |
| 4 | ROE | 0 | R06 [4]: SWD_UNDER_VOLTAGE_LOCKOUT PMIC Power On - SWD Under Voltage Lockout 0 = Normal Power On 1 = SWD Under Voltage Lockout |
| 3 | ROE | 0 | R06 [3]: SWA_OVER_VOLTAGE PMIC Power On - SWA Over Voltage 0 = Normal Power On 1 = SWA Over Voltage |
| 2 | ROE | 0 | R06 [2]: SWB_OVER_VOLTAGE PMIC Power On - SWB Over Voltage ^[3] 0 = Normal Power On 1 = SWB Over Voltage |
| 1 | ROE | 0 | R06 [1]: SWC_OVER_VOLTAGE PMIC Power On - SWC Over Voltage 0 = Normal Power On 1 = SWC Over Voltage |
| 0 | ROE | 0 | R06 [0]: SWD_OVER_VOLTAGE PMIC Power On - SWD Over Voltage 0 = Normal Power On 1 = SWD Over Voltage |

NOTE 1 The PMIC shall attempt to write this register into its non-volatile memory. However, it may not be guaranteed depending on how fast the host may shut off the input power to the PMIC. The PMIC needs minimum of 4.0V for VIN_Bulk voltage and 200 ms duration from CAMP signal assertion to guarantee the write operation into non-volatile memory.

NOTE 2 This entire register status reflects previous power down cycle of the PMIC and is updated by the PMIC on its own at each power cycle, if update is needed. Because this register is updated only if there is an update needed, there is no NVM life time impact. This register is cleared when host issues the erase command via [Table 162, Register 0x39](#). The PMIC needs minimum of 200 ms for Erase operation.

NOTE 3 The error log registers are only updated when there is a VR Disable fault when the buck regulators are under regulation. For any external command registered by the PMIC from the host (i.e., VR Disable command or CAMP assertion), followed by VIN_Bulk input supply removal to the PMIC, the PMIC does not log the error log registers.

NOTE 4 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

11.4.1 Status Registers (cont'd)

Table 112 — Register 0x07

| R07 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^{[1],[2],[3]} |
| 7 | ROE | 0 | R07 [7]: SWE_UNDER_VOLTAGE_LOCKOUT PMIC Power On - SWE Under Voltage Lockout ^[4] 0 = Normal Power On 1 = SWE Under Voltage Lockout |
| 6 | ROE | 0 | R07 [6]: SWF_UNDER_VOLTAGE_LOCKOUT PMIC Power On - SWF Under Voltage Lockout ^[5] 0 = Normal Power On 1 = SWF Under Voltage Lockout |
| 5 | ROE | 0 | R07 [5]: SWE_OVER_VOLTAGE PMIC Power On - SWE Over Voltage 0 = Normal Power On 1 = SWE Over Voltage |
| 4 | ROE | 0 | R07 [4]: SWF_OVER_VOLTAGE PMIC Power On - SWF Over Voltage 0 = Normal Power On 1 = SWF Over Voltage |
| 3:2 | RV | 0 | R07 [3:2]: Reserved |
| 1 | ROE | 0 | R07 [1]: SWE_POWER_GOOD PMIC Power On - SWE Power Not Good ^[3] 0 = Normal Power On 1 = SWE Power Not Good |
| 0 | ROE | 0 | R07 [0]: SWF_POWER_GOOD PMIC Power On - SWF Power Not Good ^[4] 0 = Normal Power On 1 = SWF Power Not Good |

- NOTE 1 The PMIC shall attempt to write this register into its non-volatile memory. However, it may not be guaranteed depending on how fast the host may shut off the input power to the PMIC. The PMIC needs minimum of 4.0V for VIN_Bulk voltage and 200 ms duration from CAMP signal assertion to guarantee the write operation into non-volatile memory.
- NOTE 2 This entire register status reflects previous power down cycle of the PMIC and is updated by the PMIC on its own at each power cycle, if update is needed. Because this register is updated only if there is an update needed, there is no NVM life time impact. This register is cleared when host issues the erase command via [Table 162, Register 0x39](#). The PMIC needs minimum of 200 ms for Erase operation.
- NOTE 3 The error log registers are only updated when there is a VR Disable fault when the buck regulators are under regulation. For any external command registered by the PMIC from the host (i.e., VR Disable command or CAMP assertion), followed by VIN_Bulk input supply removal to the PMIC, the PMIC does not log the error log registers.
- NOTE 4 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.
- NOTE 5 This register is only applicable if [Table 247, Register 0x4F](#) [6] = '0'. For any other setting in [Table 247, Register 0x4F](#) [6], this register does not apply and it is a don't care.

11.4.1 Status Registers (cont'd)

Table 113 — Register 0x08

| R08 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description |
| 7 | RO | 0 | R08 [7]: VIN_BULK_INPUT_POWER_GOOD_STATUS VIN_Bulk Input Power Good Status ^[1] 0 = Power Good 1 = Power Not Good |
| 6 | RO | 0 | R08 [6]: CRITICAL_TEMP_SHUTDOWN_STATUS Critical Temperature Shutdown Status ^[2] 0 = No Critical Temperature Shutdown 1 = Critical Temperature Shutdown |
| 5 | RO | 0 | R08 [5]: SWA_OUTPUT_POWER_GOOD_STATUS Switch Node A Output Power Good Status ^[3] 0 = Power Good 1 = Power Not Good |
| 4 | RO | 0 | R08 [4]: SWB_OUTPUT_POWER_GOOD_STATUS Switch Node B Output Power Good Status ^[4] 0 = Power Good 1 = Power Not Good |
| 3 | RO | 0 | R08 [3]: SWC_OUTPUT_POWER_GOOD_STATUS Switch Node C Output Power Good Status ^[5] 0 = Power Good 1 = Power Not Good |
| 2 | RO | 0 | R08 [2]: SWD_OUTPUT_POWER_GOOD_STATUS Switch Node D Output Power Good Status ^[6] 0 = Power Good 1 = Power Not Good |
| 1 | RO | 0 | R08 [1]: VIN_MGMT_INPUT_OVER_VOLTAGE_STATUS VIN_Mgmt Input Supply Over Voltage Status ^[7] 0 = No Over Voltage 1 = Over Voltage |
| 0 | RO | 0 | R08 [0]: VIN_BULK_INPUT_OVER_VOLTAGE_STATUS VIN_Bulk Input Supply Over Voltage Status ^[8] 0 = No Over Voltage 1 = Over Voltage |

NOTE 1 This register is set when VIN_Bulk input goes below the threshold setting in register [Table 131, Register 0x1A](#) [7:5].

NOTE 2 This register is set when PMIC temperature goes above the threshold setting in register [Table 151, Register 0x2E](#) [2:0].

NOTE 3 This register is set when SWA output voltage goes either below the threshold setting in register [Table 138, Register 0x21](#) [1:0] or above the threshold setting in register [Table 139, Register 0x22](#) [7:6].

NOTE 4 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care. This register is set when SWB output goes either below the threshold setting in register [Table 140, Register 0x23](#) [1:0] or above the threshold setting in register [Table 141, Register 0x24](#) [7:6].

NOTE 5 This register is set when SWC output goes either below the threshold setting in register [Table 142, Register 0x25](#) [1:0] or above the threshold setting in register [Table 143, Register 0x26](#) [7:6].

NOTE 6 This register is set when SWD output goes either below the threshold setting in register [Table 144, Register 0x27](#) [1:0] or above the threshold setting in register [Table 145, Register 0x28](#) [7:6].

NOTE 7 This register is set when VIN_Mgmt input voltage goes above the threshold setting in register [Table 132, Register 0x1B](#) [5].

NOTE 8 This register is set when VIN_Bulk input voltage goes above the threshold setting in register [Table 132, Register 0x1B](#) [7].

11.4.1 Status Registers (cont'd)

Table 114 — Register 0x09

| Bits | R09 | | |
|------|-----------|---------|--|
| | Attribute | Default | Description |
| 7 | RO | 0 | R09 [7]: PMIC_HIGH_TEMP_WARNING_STATUS PMIC High Temperature Warning Status ^[1] 0 = Temperature Below the Warning Threshold 1 = Temperature Exceeded the Warning Threshold |
| 6 | RO | 0 | R09 [6]: VBIAS_POWER_GOOD_STATUS VBIAS1 or VBIAS2 Power Good Status ^[2] 0 = Power Good 1 = Power Not Good |
| 5 | RO | 0 | R09 [5]: VOUT_1.8V_OUTPUT_POWER_GOOD_STATUS VOUT_1.8V LDO Output Power Good Status ^[3] 0 = Power Good 1 = Power Not Good |
| 4 | RO | 0 | R09 [4]: VIN_MGMT_TO_VIN_BULK_INPUT_SUPPLY_SWITCHOVER_STATUS VIN_Mgmt to VIN_Bulk Input Supply Automatic Switchover Status ^[4] 0 = VIN_Mgmt Input Supply is Present 1 = VIN_Mgmt Input Supply is Removed (i.e., using VIN_Bulk Input Supply) |
| 3 | RO | 0 | R09 [3]: SWA_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Switch Node A High Output Current Consumption Warning Status ^[5] 0 = No High Current Consumption Warning 1 = High Current Consumption Warning |
| 2 | RO | 0 | R09 [2]: SWB_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Switch Node B High Output Current Consumption Warning Status ^{[6],[7]} 0 = No High Current Consumption Warning 1 = High Current Consumption Warning |
| 1 | RO | 0 | R09 [1]: SWC_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Switch Node C High Output Current Consumption Warning Status ^[8] 0 = No High Current Consumption Warning 1 = High Current Consumption Warning |
| 0 | RO | 0 | R09 [0]: SWD_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Switch Node D High Output Current Consumption Warning Status ^[9] 0 = No High Current Consumption Warning 1 = High Current Consumption Warning |

NOTE 1 This register is set when PMIC temperature goes above the threshold setting in [Table 132, Register 0x1B \[2:0\]](#).

NOTE 2 This register is set when either VBias1 or VBias2 (depending on PMIC implementation) voltage goes below the threshold setting in register [Table 131, Register 0x1A \[3\]](#).

NOTE 3 This register is set when VOUT_1.8V output goes below the threshold setting in register [Table 131, Register 0x1A \[2\]](#).

NOTE 4 This register is set when VIN_Mgmt input supply goes below the threshold setting in register [Table 152, Register 0x2F \[7\]](#).

NOTE 5 This register is set when SWA output current consumption goes above the threshold setting in [Table 133, Register 0x1C \[7:0\]](#).

NOTE 6 This register is applicable regardless of the setting in [Table 247, Register 0x4F \[5,0\]](#).

NOTE 7 This register is set when SWB output current consumption goes above the threshold setting in [Table 134, Register 0x1D \[7:0\]](#). If [Table 247, Register 0x4F \[5,0\]](#) = '01', the setting in [Table 134, Register 0x1D \[7:0\]](#) and [Table 133, Register 0x1C \[7:0\]](#) must be configured identical. If [Table 247, Register 0x4F \[5,0\]](#) = '1x', the setting in [Table 134, Register 0x1D \[7:0\]](#), [Table 133, Register 0x1C \[7:0\]](#) and [Table 182, Register 0x11A \[7:0\]](#) must be configured identical.

NOTE 8 This register is set when SWC output current consumption goes above the threshold setting in [Table 135, Register 0x1E \[7:0\]](#). If [Table 247, Register 0x4F \[6\]](#) = '1', the setting in [Table 135, Register 0x1E \[7:0\]](#) and [Table 183, Register 0x11B \[7:0\]](#) must be configured identical.

NOTE 9 This register is set when SWD output current consumption goes above the threshold setting in [Table 136, Register 0x1F \[7:0\]](#).

11.4.1 Status Registers (cont'd)

Table 115 — Register 0x0A

| Bits | R0A | | |
|------|-----------|---------|---|
| | Attribute | Default | Description |
| 7 | RO | 0 | R0A [7]: SWA_OUTPUT_OVER_VOLTAGE_STATUS Switch Node A Output Over Voltage Status ^[1] 0 = No Over Voltage 1 = Over Voltage |
| 6 | RO | 0 | R0A [6]: SWB_OUTPUT_OVER_VOLTAGE_STATUS Switch Node B Output Over Voltage Status ^[2] 0 = No Over Voltage 1 = Over Voltage |
| 5 | RO | 0 | R0A [5]: SWC_OUTPUT_OVER_VOLTAGE_STATUS Switch Node C Output Over Voltage Status ^[3] 0 = No Over Voltage 1 = Over Voltage |
| 4 | RO | 0 | R0A [4]: SWD_OUTPUT_OVER_VOLTAGE_STATUS Switch Node D Output Over Voltage Status ^[4] 0 = No Over Voltage 1 = Over Voltage |
| 3 | RO | 0 | R0A [3]: PEC_ERROR_STATUS Packet Error Code Status ^{[5],[6]} 0 = No PEC Error 1 = PEC Error |
| 2 | RO | 0 | R0A [2]: PARITY_ERROR_STATUS T Bit Parity Error Status ^{[5],[7]} 0 = No Parity Error 1 = Parity Error |
| 1 | RO | 0 | R0A [1]: IBI_AND_GLOBAL_STATUS In Band Interrupt and Global Status ^[8] 0 = No Pending IBI or Outstanding Status 1 = Pending IBI or Outstanding Status |
| 0 | RV | 0 | R0A [0]: Reserved |

NOTE 1 This register is set when SWA output voltage goes above the threshold setting in [Table 139, Register 0x22](#) [5:4].

NOTE 2 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care. This register is set when SWB output voltage goes above the threshold setting in [Table 141, Register 0x24](#) [5:4].

NOTE 3 This register is set when SWC output voltage goes above the threshold setting in [Table 143, Register 0x26](#) [5:4].

NOTE 4 This register is set when SWD output voltage goes above the threshold setting in [Table 145, Register 0x28](#) [5:4].

NOTE 5 Applicable in I3C Basic Mode Only and if enabled in register [Table 158, Register 0x34](#) [7].

NOTE 6 This register is updated when PMIC device goes through bus reset as described in clause 7.8.

NOTE 7 Applicable in I3C Basic Mode and if enabled in register [Table 158, Register 0x34](#) [5]. Also applicable in I²C mode for supported CCC.

NOTE 8 This register can be used as Global Status in addition to IBI status. When IBI function is enabled, this register is automatically cleared when PMIC transmits IBI payload; however individual status registers still require an explicit clear command from host.

11.4.1 Status Registers (cont'd)

Table 116 — Register 0x0B

| Bits | R0B | | |
|------|-----------|---------|---|
| | Attribute | Default | Description |
| 7 | RO | 0 | R0B [7]: SWA_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node A Output Current Limiter Warning Status ^[1] 0 = No Current Limiter Event 1 = Current Limiter Event |
| 6 | RO | 0 | R0B [6]: SWB_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node B Output Current Limiter Warning Status ^[2] 0 = No Current Limiter Event 1 = Current Limiter Event |
| 5 | RO | 0 | R0B [5]: SWC_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node C Output Current Limiter Warning Status 0 = No Current Limiter Event 1 = Current Limiter Event |
| 4 | RO | 0 | R0B [4]: SWD_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node D Output Current Limiter Warning Status ^[3] 0 = No Current Limiter Event 1 = Current Limiter Event |
| 3 | RO | 0 | R0B [3]: SWA_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node A Output Under Voltage Lockout Status ^[4] 0 = No Under Voltage Lockout 1 = Under Voltage Lockout |
| 2 | RO | 0 | R0B [2]: SWB_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node B Output Under Voltage Lockout Status ^[5] 0 = No Under Voltage Lockout 1 = Under Voltage Lockout |
| 1 | RO | 0 | R0B [1]: SWC_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node C Output Under Voltage Lockout Status 0 = No Under Voltage Lockout 1 = Under Voltage Lockout |
| 0 | RO | 0 | R0B [0]: SWD_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node D Output Under Voltage Lockout Status ^[6] 0 = No Under Voltage Lockout 1 = Under Voltage Lockout |

NOTE 1 This register is set when SWA output current goes above the threshold setting in [Table 137, Register 0x20](#) [7:6].

NOTE 2 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [5,0]. This register is set when SWB output current goes above the threshold setting in [Table 137, Register 0x20](#) [5:4]. If [Table 247, Register 0x4F](#) [5,0] = '01', the setting in [Table 137, Register 0x20](#) [5:4] must be identical as [Table 137, Register 0x20](#) [7:6]. If [Table 247, Register 0x4F](#) [5,0] = '1x', the setting in [Table 137, Register 0x20](#) [5:4], [Table 137, Register 0x20](#) [7:6] and [Table 184, Register 0x11C](#) [7:6] must be configured identical.

NOTE 3 This register is set when SWD output current goes above the threshold setting in [Table 137, Register 0x20](#) [1:0].

NOTE 4 This register is set when SWA output voltage goes below the threshold setting in [Table 139, Register 0x22](#) [3:2].

NOTE 5 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care. This register is set when SWB output voltage goes below the threshold setting in [Table 141, Register 0x24](#) [3:2].

NOTE 6 This register is set when SWD output voltage goes below the threshold setting in [Table 145, Register 0x28](#) [3:2].

11.4.1 Status Registers (cont'd)

Table 117 — Register 0x0C

| R0C | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7:0 | RO | - | <p>R0C [7:0]: SWA_OUTPUT_CURRENT_POWER_MEASUREMENT Switch Node A Output Current or Output Power^[3] Measurement^[4]</p> <p>If Table 131, Register 0x1A [1] = '0':</p> <p>0000 0000 = Undefined 0000 0001 = 125 mA or 125 mW 0000 0010 = 250 mA or 250 mW ... 1111 1111 \geq 31.875 A or 31.875 W</p> <p>If Table 131, Register 0x1A [1] = '1':</p> <p>Sum of SWA, SWB, SWC and SWD Output Power^[5]</p> <p>0000 0000 = Undefined 0000 0001 = 125 mW 0000 0010 = 250 mW ... 1111 1111 \geq 31.875 W</p> |

NOTE 1 This register is only applicable if [Table 155, Register 0x32](#) [1:0] = '00'

NOTE 2 The PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers VR Disable command, PMIC does not report current or power measurement and register content may have stale data. For all other events that causes PMIC's power good status as Not Good, the PMIC continues to provide current or power measurement.

NOTE 3 If [Table 132, Register 0x1B](#) [6] = '0', the PMIC reports current measurement. If [Table 132, Register 0x1B](#) [6] = '1', the PMIC reports power measurement.

NOTE 4 If [Table 247, Register 0x4F](#) [5,0] = '01', host adds the current or power reported in [Table 117, Register 0x0C](#) [7:0] and [Table 118, Register 0x0D](#) [7:0] for total current or power consumption. If [Table 247, Register 0x4F](#) [5,0] = '1x', this register does not apply; the host shall set [Table 155, Register 0x32](#) [1:0] = '01' and read from registers [Table 167, Register 0x100](#) to [Table 174, Register 0x107](#).

NOTE 5 Register [Table 132, Register 0x1B](#) [6] must be configured as '1'.

11.4.1 Status Registers (cont'd)

Table 118 — Register 0x0D

| R0D | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7:0 | RO | - | <p>R0D [7:0]: SWB_OUTPUT_CURRENT_POWER_MEASUREMENT Switch Node B Output Current or Output Power^[3] Measurement^[4]</p> <p>If Table 131, Register 0x1A[1] = '0': 0000 0000 = Undefined 0000 0001 = 125 mA or 125 mW 0000 0010 = 250 mA or 250 mW .. 1111 1111 \geq 31.875 A or 31.875 W</p> |

NOTE 1 This register is only applicable if [Table 155, Register 0x32](#) [1:0] = '00'

NOTE 2 The PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers VR Disable command, PMIC does not report current or power measurement and register content may have stale data. For all other events that causes PMIC's power good status as Not Good, the PMIC continues to provide current or power measurement.

NOTE 3 If [Table 132, Register 0x1B](#) [6] = '0', the PMIC reports current measurement. If [Table 132, Register 0x1B](#) [6] = '1', the PMIC reports power measurement.

NOTE 4 If [Table 247, Register 0x4F](#) [5,0] = '01', host adds the current or power reported in [Table 117, Register 0x0C](#) [7:0] and [Table 118, Register 0x0D](#) [7:0] for total current or power consumption. If [Table 247, Register 0x4F](#) [5,0] = '1x', this register does not apply; the host shall set [Table 155, Register 0x32](#) [1:0] = '01' and read from registers [Table 167, Register 0x100](#) to [Table 174, Register 0x107](#).

Table 119 — Register 0x0E

| R0E | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7:0 | RO | - | <p>R0E [7:0]: SWC_OUTPUT_CURRENT_POWER_MEASUREMENT Switch Node C Output Current or Output Power^[3] Measurement^[4]</p> <p>If Table 131, Register 0x1A[1] = '0': 0000 0000 = Undefined 0000 0001 = 125 mA or 125 mW 0000 0010 = 250 mA or 250 mW .. 1111 1111 \geq 31.875 A or 31.875 W</p> |

NOTE 1 This register is only applicable if [Table 155, Register 0x32](#) [1:0] = '00'

NOTE 2 The PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers VR Disable command, PMIC does not report current or power measurement and register content may have stale data. For all other events that causes PMIC's power good status as Not Good, the PMIC continues to provide current or power measurement.

NOTE 3 If [Table 132, Register 0x1B](#) [6] = '0', the PMIC reports current measurement. If [Table 132, Register 0x1B](#) [6] = '1', the PMIC reports power measurement.

NOTE 4 If [Table 247, Register 0x4F](#) [6] = '1', this register does not apply; the host shall set [Table 155, Register 0x32](#) [1:0] = '01' and read from registers [Table 167, Register 0x100](#) to [Table 174, Register 0x107](#).

11.4.1 Status Registers (cont'd)

Table 120 — Register 0x0F

| R0F | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7:0 | RO | - | <p>R0F [7:0]: SWD_OUTPUT_CURRENT_POWER_MEASUREMENT Switch Node D Output Current or Output Power^[3] Measurement</p> <p>If Table 131, Register 0x1A [1] = '0': 0000 0000 = Undefined 0000 0001 = 125 mA or 125 mW 0000 0010 = 250 mA or 250 mW .. 1111 1111 ≥ 31.875 A or 31.875 W</p> |

NOTE 1 This register is only applicable if [Table 155, Register 0x32](#) [1:0] = '00'

NOTE 2 The PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers VR Disable command, PMIC does not report current or power measurement and register content may have stale data. For all other events that causes PMIC's power good status as Not Good, the PMIC continues to provide current or power measurement.

NOTE 3 If [Table 132, Register 0x1B](#) [6] = '0', the PMIC reports current measurement. If [Table 132, Register 0x1B](#) [6] = '1', the PMIC reports power measurement.

11.4.2 Clear Registers

For each Real Time Status Registers ([Table 113, Register 0x08](#) [7:0], [Table 114, Register 0x09](#) [7:0], [Table 115, Register 0x0A](#) [7:1], [Table 116, Register 0x0B](#) [7:0], [Table 157, Register 0x33](#) [4:2], [Table 175, Register 0x108](#) [7:0] and [Table 176, Register 0x109](#) [7:6]), the PMIC offers a way to clear the status of each event. The clear registers are [Table 121, Register 0x10](#) [7,5:0], [Table 122, Register 0x11](#) [7:0], [Table 123, Register 0x12](#) [7:2], [Table 124, Register 0x13](#) [7:0], [Table 125, Register 0x14](#) [4:2,0], [Table 178, Register 0x10E](#) [7:0] and [Table 179, Register 0x10F](#) [7:6] respectively. All clear registers are Write '1' only registers. When '1' is written to any of the clear registers, the PMIC updates the status registers to default state and removes the interrupt condition on GSI_n and PWR_GOOD output signal assuming that event is no longer present. If the failing condition is still present, the status register will still remain at '1'. Note that GSI_n and PWR_GOOD interrupt is only applicable if that event is not masked. GSI_n output signal can be disabled.

When '1' is written to any of the clear registers, there are three categories of response by the PMIC.

1. PMIC removes GSI_n interrupt (PWR_GOOD interrupt is not applicable. Related status registers are: [Table 121, Register 0x10](#) [1], [Table 122, Register 0x11](#) [7,4:0], [Table 124, Register 0x13](#) [7:4], [Table 125, Register 0x14](#) [4], [Table 178, Register 0x10E](#) [5:4, 1:0].
2. PMIC removes GSI_n and PWR_GOOD interrupt. Related status registers are: [Table 121, Register 0x10](#) [7,5:2], [Table 122, Register 0x11](#) [6:5], [Table 125, Register 0x14](#) [2], [Table 178, Register 0x10E](#) [7:6].
3. PMIC only removes GSI_n interrupt and does not remove PWR_GOOD interrupt. Related status registers are: [Table 121, Register 0x10](#) [0], [Table 123, Register 0x12](#) [7:4], [Table 124, Register 0x13](#) [3:0], [Table 125, Register 0x14](#) [3], [Table 178, Register 0x10E](#) [3:2], [Table 179, Register 0x10F](#) [7:6].
The host is expected to either power cycle the PMIC or re-issue the VR Enable command if PMIC is in non write-protect mode.

The PMIC offers a Global Clear command by writing '1' to registers [Table 125, Register 0x14](#) [0]. This command works same way as individual clear command. This command can alternatively be used by the host if more than one clear command is required to different registers.

11.4.2 Clear Registers (cont'd)

Table 121 — Register 0x10

| R10 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description ^[1] |
| 7 | 1O | 0 | R10 [7]: CLEAR_VIN_BULK_INPUT_POWER_GOOD_STATUS Clear VIN_Bulk Input Power Good Status. 1 = Clear Register Table 113, Register 0x08 [7] ^[2] |
| 6 | RV | 0 | R10 [6]: Reserved |
| 5 | 1O | 0 | R10 [5]: CLEAR_SWA_OUTPUT_POWER_GOOD_STATUS Clear SWA Output Power Good Status. 1 = Clear Register Table 113, Register 0x08 [5] ^[2] |
| 4 | 1O | 0 | R10 [4]: CLEAR_SWB_OUTPUT_POWER_GOOD_STATUS Clear SWB Output Power Good Status. ^[3] 1 = Clear Register Table 113, Register 0x08 [4] ^[2] |
| 3 | 1O | 0 | R10 [3]: CLEAR_SWC_OUTPUT_POWER_GOOD_STATUS Clear SWC Output Power Good Status. 1 = Clear Register Table 113, Register 0x08 [3] ^[2] |
| 2 | 1O | 0 | R10 [2]: CLEAR_SWD_OUTPUT_POWER_GOOD_STATUS Clear SWD Output Power Good Status. 1 = Clear Register Table 113, Register 0x08 [2] ^[2] |
| 1 | 1O | 0 | R10 [1]: CLEAR_VIN_MGMT_INPUT_OVER_VOLTAGE_STATUS Clear VIN_Mgmt Input Supply Over Voltage Status. 1 = Clear Register Table 113, Register 0x08 [1] ^[2] |
| 0 | 1O | 0 | R10 [0]: CLEAR_VIN_BULK_INPUT_OVER_VOLTAGE_STATUS Clear VIN_Bulk Input Supply Over Voltage Status. 1 = Clear Register Table 113, Register 0x08 [0] ^[2] |

NOTE 1 [Table 121, Register 0x10](#) [7:0] bits are self-clearing.

NOTE 2 See [Table 28](#) and [Table 29](#) for GSI_n and POWER_GOOD output signal status change.

NOTE 3 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

11.4.2 Clear Registers (cont'd)

Table 122 — Register 0x11

| R11 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^[1] |
| 7 | 10 | 0 | R11 [7]: CLEAR_PMIC_HIGH_TEMP_WARNING_STATUS Clear PMIC High Temperature Warning Status. 1 = Clear Register Table 114, Register 0x09 [7] ^[2] |
| 6 | 10 | 0 | R11 [6]: CLEAR_VBIAS_POWER_GOOD_STATUS Clear VBIAS (applies to both VBIAS1 and VBIAS2) Power Good Status. 1 = Clear Register Table 114, Register 0x09 [6] ^[2] |
| 5 | 10 | 0 | R11 [5]: CLEAR_VOUT_1.8V_OUTPUT_POWER_GOOD_STATUS Clear VOUT_1.8V Output Power Good Status. 1 = Clear Register Table 114, Register 0x09 [5] ^[2] |
| 4 | 10 | 0 | R11 [4]: CLEAR_VIN_MGMT_TO_VIN_BULK_INPUT_SWITCHOVER_STATUS Clear VIN_Mgmt to VIN_Bulk Input Supply Switchover Status. 1 = Clear Register Table 114, Register 0x09 [4] ^[2] |
| 3 | 10 | 0 | R11 [3]: CLEAR_SWA_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Clear Switch Node A High Output Current Consumption Warning Status. 1 = Clear Register Table 114, Register 0x09 [3] ^[2] |
| 2 | 10 | 0 | R11 [2]: CLEAR_SWB_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Clear Switch Node B High Output Current Consumption Warning Status. ^[3] Clear Register Table 114, Register 0x09 [2] ^[2] |
| 1 | 10 | 0 | R11 [1]: CLEAR_SWC_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Clear Switch Node C High Output Current Consumption Warning Status. ^[4] 1 = Clear Register Table 114, Register 0x09 [1] ^[2] |
| 0 | 10 | 0 | R11 [0]: CLEAR_SWD_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Clear Switch Node D High Output Current Consumption Warning Status. 1 = Clear Register Table 114, Register 0x09 [0] ^[2] |

NOTE 1 [Table 122, Register 0x11](#) [7:0] bits are self-clearing.

NOTE 2 See [Table 28](#) and [Table 29](#) for GSI_n and POWER_GOOD output signal status change.

NOTE 3 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [5,0].

NOTE 4 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [6].

11.4.2 Clear Registers (cont'd)

Table 123 — Register 0x12

| R12 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description ^[1] |
| 7 | 1O | 0 | R12 [7]: CLEAR_SWA_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node A Output Over Voltage Status. 1 = Clear Register Table 115, Register 0x0A [7] ^[2] |
| 6 | 1O | 0 | R12 [6]: CLEAR_SWB_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node B Output Over Voltage Status. ^[3] 1 = Clear Register Table 115, Register 0x0A [6] ^[2] |
| 5 | 1O | 0 | R12 [5]: CLEAR_SWC_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node C Output Over Voltage Status. 1 = Clear Register Table 115, Register 0x0A [5] ^[2] |
| 4 | 1O | 0 | R12 [4]: CLEAR_SWD_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node D Output Over Voltage Status. 1 = Clear Register Table 115, Register 0x0A [4] ^[2] |
| 3 | 1O | 0 | R12 [3]: CLEAR_PEC_ERROR_STATUS Clear PEC Error Status. 1 = Clear Register Table 115, Register 0x0A [3] |
| 2 | 1O | 0 | R12 [2]: CLEAR_PARITY_ERROR_STATUS Clear Parity Error Status. 1 = Clear Register Table 115, Register 0x0A [2] |
| 1:0 | RV | 0 | R12 [1:0]: Reserved |

NOTE 1 [Table 123, Register 0x12](#) [7:0] are self-clearing bits.

NOTE 2 See [Table 28](#) and [Table 29](#) for GSI_n and POWER_GOOD output signal status change.

NOTE 3 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

11.4.2 Clear Registers (cont'd)

Table 124 — Register 0x13

| R13 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description ^[1] |
| 7 | 10 | 0 | R13 [7]: CLEAR_SWA_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Clear Switch Node A Output Current Limiter Warning Status. 1 = Clear Register Table 116, Register 0x0B [7] ^[2] |
| 6 | 10 | 0 | R13 [6]: CLEAR_SWB_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Clear Switch Node B Output Current Limiter Warning Status. ^[3] 1 = Clear Register Table 116, Register 0x0B [6] ^[2] |
| 5 | 10 | 0 | R13 [5]: CLEAR_SWC_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Clear Switch Node C Output Current Limiter Warning Status. ^[4] 1 = Clear Register Table 116, Register 0x0B [5] ^[2] |
| 4 | 10 | 0 | R13 [4]: CLEAR_SWD_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Clear Switch Node D Output Current Limiter Warning Status. 1 = Clear Register Table 116, Register 0x0B [4] ^[2] |
| 3 | 10 | 0 | R13 [3]: CLEAR_SWA_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Clear Switch Node A Output Under Voltage Lockout Status. 1 = Clear Register Table 116, Register 0x0B [3] ^[2] |
| 2 | 10 | 0 | R13 [2]: CLEAR_SWB_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Clear Switch Node B Output Under Voltage Lockout Status. ^[5] 1 = Clear Register Table 116, Register 0x0B [2] ^[2] |
| 1 | 10 | 0 | R13 [1]: CLEAR_SWC_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Clear Switch Node C Output Under Voltage Lockout Status. 1 = Clear Register Table 116, Register 0x0B [1] ^[2] |
| 0 | 10 | 0 | R13 [0]: CLEAR_SWD_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Clear Switch Node D Output Under Voltage Lockout Status. 1 = Clear Register Table 116, Register 0x0B [0] ^[2] |

NOTE 1 [Table 124, Register 0x13](#) [7:0] bits self-clearing.

NOTE 2 See [Table 28](#) and [Table 29](#) for GSI_n and POWER_GOOD output signal status change.

NOTE 3 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [5,0].

NOTE 4 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [6].

NOTE 5 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

11.4.2 Clear Registers (cont'd)

Table 125 — Register 0x14

| R14 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description ^[1] |
| 7:5 | RV | 0 | R14 [7:5]: Reserved |
| 4 | 1O | 0 | R14 [4]: CLEAR_VIN_MGMT_POWER_GOOD_STATUS_SWITCHOVER_MODE Clear Valid VIN_Mgmt Power Good Status in Switchover Mode. 1 = Clear Register Table 157, Register 0x33 [4] ^[2] |
| 3 | 1O | 0 | R14 [3]: CLEAR_VBIAS_OUTPUT_OR_VIN_BULK_UNDER_VOLTAGE_LOCKOUT_STATUS Clear VBias Output or VIN_Bulk Input Under Voltage Lockout Status. 1 = Clear Register Table 157, Register 0x33 [3] ^[2] |
| 2 | 1O | 0 | R14 [2]: CLEAR_VOUT_1.0V_OUTPUT_POWER_GOOD_STATUS Clear VOUT_1.0V Output Power Good Status. 1 = Clear Register Table 157, Register 0x33 [2] ^[2] |
| 1 | RV | 0 | R14 [1]: Reserved |
| 0 | 1O | 0 | R14 [0]: GLOBAL_CLEAR_STATUS Clear all ^[3] status bits. 1 = Clear all status bits ^[4] |

NOTE 1 [Table 125, Register 0x14](#) [4:2, 0] bits are self-clearing.

NOTE 2 See [Table 28](#) and [Table 29](#) for GSI_n and POWER_GOOD output signal status change.

NOTE 3 All status bits in register [Table 121, Register 0x10](#) [7:5:0], [Table 122, Register 0x11](#) [7:0], [Table 123, Register 0x12](#) [7:2], [Table 124, Register 0x13](#) [7:0], [Table 125, Register 0x14](#) [4:2], [Table 178, Register 0x10E](#) [7:0] and [Table 179, Register 0x10F](#) [7:6,0].

NOTE 4 See [Table 28](#) and [Table 29](#) for GSI_n and POWER_GOOD output signal status change.

11.4.3 Mask Registers

For each Real Time Status Registers ([Table 113, Register 0x08 \[7:0\]](#), [Table 114, Register 0x09 \[7:0\]](#), [Table 115, Register 0x0A \[7:1\]](#), [Table 116, Register 0x0B \[7:0\]](#), [Table 157, Register 0x33 \[4:2\]](#), [Table 175, Register 0x108 \[7:0\]](#) and [Table 176, Register 0x109 \[7:6\]](#)), the PMIC offers a way to mask the status of each event interrupt. The mask registers are [Table 126, Register 0x15 \[7,5:0\]](#), [Table 127, Register 0x16 \[7:0\]](#), [Table 128, Register 0x17 \[7:2\]](#), [Table 129, Register 0x18 \[7:0\]](#), [Table 130, Register 0x19 \[4:2\]](#), [Table 180, Register 0x114 \[7:0\]](#) and [Table 181, Register 0x115 \[7:6\]](#) respectively. The mask registers only mask the event interrupt on GSI_n and PWR_GOOD signal.

There is also a global mask bits register control [Table 152, Register 0x2F \[1:0\]](#) to control the GSI_n and PWR_GOOD output signal. When all mask registers are [Table 126, Register 0x15 \[7,5:0\]](#), [Table 127, Register 0x16 \[7:0\]](#), [Table 128, Register 0x17 \[7:2\]](#), [Table 129, Register 0x18 \[7:0\]](#), [Table 130, Register 0x19 \[4:2\]](#), [Table 180, Register 0x114 \[7:0\]](#) and [Table 181, Register 0x115 \[7:6\]](#) configured as '0', the setting in [Table 152, Register 0x2F \[1:0\]](#) does not matter. The setting in [Table 152, Register 0x2F \[1:0\]](#) only matters when one or more mask registers [Table 126, Register 0x15 \[7,5:0\]](#), [Table 127, Register 0x16 \[7:0\]](#), [Table 128, Register 0x17 \[7:2\]](#), [Table 129, Register 0x18 \[7:0\]](#), [Table 130, Register 0x19 \[4:2\]](#), [Table 180, Register 0x114 \[7:0\]](#) and [Table 181, Register 0x115 \[7:6\]](#) are configured to '1'.

For any failure events that causes the PMIC to generate VR Disable command on its own, the mask register bits ([Table 126, Register 0x15 \[0\]](#), [Table 128, Register 0x17 \[7:4\]](#), [Table 129, Register 0x18 \[3:0\]](#), [Table 130, Register 0x19 \[3\]](#), [Table 152, Register 0x2F \[1:0\]](#), [Table 180, Register 0x114 \[3:2\]](#), [Table 181, Register 0x115 \[7:6\]](#)) do not apply and PMIC will assert PWR_GOOD output signal regardless of the setting in mask registers. The PMIC still updates the status registers appropriately when any event occurs. When masked, the host is expected to read the status registers periodically to learn if any of the events have occurred or not. The host can mask or unmask each event individually. The host can mask or unmask at any time in non write-protect mode. In write-protect mode of operation, the mask registers are locked.

11.4.3 Mask Registers (cont'd)

Table 126 — Register 0x15

| Bits | R15 | | |
|------|-----------|---------|---|
| | Attribute | Default | Description |
| 7 | RW | 1 | R15 [7]: MASK_VIN_BULK_INPUT_POWER_GOOD_STATUS Mask VIN_Bulk Input Power Good Status Event. 0 = Do Not Mask VIN_Bulk Input Power Good Status Event 1 = Mask VIN_Bulk Input Power Good Status Event ^[1] |
| 6 | RV | 0 | R15 [6]: Reserved |
| 5 | RW | 1 | R15 [5]: MASK_SWA_OUTPUT_POWER_GOOD_STATUS Mask SWA Output Power Good Status Event. 0 = Do Not Mask SWA Output Power Good Status Event 1 = Mask SWA Output Power Good Status Event ¹ |
| 4 | RW | 1 | R15 [4]: MASK_SWB_OUTPUT_POWER_GOOD_STATUS Mask SWB Output Power Good Status Event. ^[2] 0 = Do Not Mask SWB Output Power Good Status Event 1 = Mask SWB Output Power Good Status Event ¹ |
| 3 | RW | 1 | R15 [3]: MASK_SWC_OUTPUT_POWER_GOOD_STATUS Mask SWC Output Power Good Status Event. 0 = Do Not Mask SWC Output Power Good Status Event 1 = Mask SWC Output Power Good Status Event ¹ |
| 2 | RW | 1 | R15 [2]: MASK_SWD_OUTPUT_POWER_GOOD_STATUS Mask SWD Output Power Good Status Event. 0 = Do Not Mask SWD Output Power Good Status Event 1 = Mask SWD Output Power Good Status Event ¹ |
| 1 | RW | 0 | R15 [1]: MASK_VIN_MGMT_INPUT_OVER_VOLTAGE_STATUS Mask VIN_Mgmt Input Supply Over Voltage Status Event. 0 = Do Not Mask VIN_Mgmt Input Supply Over Voltage Status Event 1 = Mask VIN_Mgmt Input Supply Over Voltage Status Event ^[3] |
| 0 | RW | 0 | R15 [0]: MASK_VIN_BULK_INPUT_OVER_VOLTAGE_STATUS Mask VIN_Bulk Input Supply Over Voltage Status Event. 0 = Do Not Mask VIN_Bulk Input Supply Over Voltage Status Event 1 = Mask VIN_Bulk Input Supply Over Voltage Status Event ³ |

NOTE 1 Not assert GSI_n or assert POWER_GOOD output signal.

NOTE 2 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 3 Not assert GSI_n output signal.

11.4.3 Mask Registers (cont'd)

Table 127 — Register 0x16

| R16 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description |
| 7 | RW | 0 | R16 [7]: MASK_PMIC_HIGH_TEMP_WARNING_STATUS Mask PMIC High Temperature Warning Status Event. 0 = Do Not Mask PMIC High Temperature Warning Status Event 1 = Mask PMIC High Temperature Warning Status Event ^[1] |
| 6 | RW | 0 | R16 [6]: MASK_VBIAS_POWER_GOOD_STATUS Mask VBIAS (applies to both VBIAS1 and VBIAS2) Power Good Status Event. 0 = Do Not Mask VBIAS Power Good Status Event 1 = Mask VBIAS Power Good Status Event ^[2] |
| 5 | RW | 1 | R16 [5]: MASK_VOUT_1.8V_OUTPUT_POWER_GOOD_STATUS Mask VOUT_1.8V Output Power Good Status Event. 0 = Do Not Mask 1.8V Output Power Good Status Event 1 = Mask 1.8V Output Power Good Status Event ² |
| 4 | RW | 0 | R16 [4]: MASK_VIN_MGMT_TO_VIN_BULK_SWITCHOVER_STATUS Mask VIN_Mgmt to VIN_Bulk Input Supply Switchover Status Event. 0 = Do Not Mask VIN_Mgmt to VIN_Bulk Input Supply Switchover Status Event 1 = Mask VIN_Mgmt to VIN_Bulk Input Supply Switchover Status Event ¹ |
| 3 | RW | 0 | R16 [3]: MASK_SWA_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Mask SWA High Output Current Consumption Warning Status Event. 0 = Do Not Mask SWA Output Current Consumption Warning Status Event 1 = Mask SWA Output Current Consumption Warning Status Event ¹ |
| 2 | RW | 0 | R16 [2]: MASK_SWB_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Mask SWB High Output Current Consumption Warning Status Event. ^[3] 0 = Do Not Mask SWB Output Current Consumption Warning Status Event 1 = Mask SWB Output Current Consumption Warning Status Event ¹ |
| 1 | RW | 0 | R16 [1]: MASK_SWC_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Mask SWC High Output Current Consumption Warning Status Event. ^[4] 0 = Do Not Mask SWC Output Current Consumption Warning Status Event 1 = Mask SWC Output Current Consumption Warning Status Event ¹ |
| 0 | RW | 0 | R16 [0]: MASK_SWD_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Mask SWD High Output Current Consumption Warning Status Event. 0 = Do Not Mask SWD Output Current Consumption Warning Status Event 1 = Mask SWD Output Current Consumption Warning Status Event ¹ |

NOTE 1 Not assert GSI_n output signal.

NOTE 2 Not assert GSI_n or assert POWER_GOOD output signal

NOTE 3 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [5,0].

NOTE 4 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [6].

11.4.3 Mask Registers (cont'd)

Table 128 — Register 0x17

| R17 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description |
| 7 | RW | 0 | R17 [7]: MASK_SWA_OUTPUT_OVER_VOLTAGE_STATUS Mask SWA Output Over Voltage Status Event. 0 = Do Not Mask SWA Output Over Voltage Status Event 1 = Mask SWA Output Over Voltage Status Event ^[1] |
| 6 | RW | 0 | R17 [6]: MASK_SWB_OUTPUT_OVER_VOLTAGE_STATUS Mask SWB Output Over Voltage Status Event. ^[2] 0 = Do Not Mask SWB Output Over Voltage Status Event 1 = Mask SWB Output Over Voltage Status Event ¹ |
| 5 | RW | 0 | R17 [5]: MASK_SWC_OUTPUT_OVER_VOLTAGE_STATUS Mask SWC Output Over Voltage Status Event. 0 = Do Not Mask SWC Output Over Voltage Status Event 1 = Mask SWC Output Over Voltage Status Event ¹ |
| 4 | RW | 0 | R17 [4]: MASK_SWD_OUTPUT_OVER_VOLTAGE_STATUS Mask SWD Output Over Voltage Status Event. 0 = Do Not Mask SWD Output Over Voltage Status Event 1 = Mask SWD Output Over Voltage Status Event ¹ |
| 3 | RW | 0 | R17 [3]: MASK_PEC_ERROR_STATUS Mask PEC Error Event for GSI_n output Only ^[3] 0 = Do Not Mask PEC Error Status Event 1 = Mask PEC Error Status |
| 2 | RW | 0 | R17 [2]: MASK_PARITY_ERROR_STATUS Mask Parity Error Event for GSI_n output Only ³ 0 = Do Not Mask Parity Error Status Event 1 = Mask Parity Error Status |
| 1:0 | RV | 0 | R17 [1:0]: Reserved |

NOTE 1 Not assert GSI_n output signal.

NOTE 2 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 3 Only applicable when PMIC is in I3C Basic Mode. This Mask register only masks the GSI_n output. Does not apply to IBI.

11.4.3 Mask Registers (cont'd)

Table 129 — Register 0x18

| R18 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description |
| 7 | RW | 0 | R18 [7]: MASK_SWA_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Mask SWA Output Current Limiter Warning Status Event. 0 = Do Not Mask SWA Output Current Limiter Warning Status Event 1 = Mask SWA Output Current Limiter Warning Status Event ^[1] |
| 6 | RW | 0 | R18 [6]: MASK_SWB_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Mask SWB Output Current Limiter Warning Status Event. ^[2] 0 = Do Not Mask SWB Output Current Limiter Warning Status Event 1 = Mask SWB Output Current Limiter Warning Status Event ¹ |
| 5 | RW | 0 | R18 [5]: MASK_SWC_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Mask SWC Output Current Limiter Warning Status Event. 0 = Do Not Mask SWC Output Current Limiter Warning Status Event 1 = Mask SWC Output Current Limiter Warning Status Event ¹ |
| 4 | RW | 0 | R18 [4]: MASK_SWD_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Mask SWD Output Current Limiter Warning Status Event. 0 = Do Not Mask SWD Output Current Limiter Warning Status Event 1 = Mask SWD Output Current Limiter Warning Status Event ¹ |
| 3 | RW | 0 | R18 [3]: MASK_SWA_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Mask SWA Output Under Voltage Lockout Status Event. 0 = Do Not Mask SWA Output Under Voltage Lockout Status Event 1 = Mask SWA Output Under Voltage Lockout Status Event ¹ |
| 2 | RW | 0 | R18 [2]: MASK_SWB_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Mask SWB Output Under Voltage Lockout Status Event. ^[3] 0 = Do Not Mask SWB Output Under Voltage Lockout Status Event 1 = Mask SWB Output Under Voltage Lockout Status Event ¹ |
| 1 | RW | 0 | R18 [1]: MASK_SWC_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Mask SWC Output Under Voltage Lockout Status Event. 0 = Do Not Mask SWC Output Under Voltage Lockout Status Event 1 = Mask SWC Output Under Voltage Lockout Status Event ¹ |
| 0 | RW | 0 | R18 [0]: MASK_SWD_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Mask SWD Output Under Voltage Lockout Status Event. 0 = Do Not Mask SWD Output Under Voltage Lockout Status Event 1 = Mask SWD Output Under Voltage Lockout Status Event ¹ |

NOTE 1 Not assert GSI_n output signal.

NOTE 2 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [5,0].

NOTE 3 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

11.4.3 Mask Registers (cont'd)

Table 130 — Register 0x19

| R19 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description |
| 7:5 | RV | 0 | R19 [7:5]: Reserved |
| 4 | RW | 0 | R19 [4]: MASK_VIN_MGMT_POWER_GOOD_STATUS_SWITCHOVER_MODE Mask VIN_Mgmt Input Supply Power Good Status in Switchover Mode Only 0 = Do Not Mask VIN_Mgmt Input Power Supply Power Good Status Event in Switchover Mode 1 = Mask VIN_Mgmt Input Power Supply Power Good Status Event in Switchover Mode ^[1] |
| 3 | RW | 0 | R19 [3]: MASK_VBIAS_OUTPUT_OR_VIN_BULK_UNDER_VOLTAGE_LOCKOUT_STATUS Mask VBIAS Output or VIN_Bulk Input Under Voltage Lockout Event 0 = Do Not Mask Vbias Output or VIN_Bulk Input Under Voltage Lockout Event 1 = Mask Vbias Output or VIN_Bulk Input Under Voltage Lockout Event ¹ |
| 2 | RW | 1 | R19 [2]: MASK_VOUT_1.0V_OUTPUT_POWER_GOOD_STATUS Mask VOUT_1.0V Output Power Good Status Event. 0 = Do Not Mask VOUT_1.0V Output Power Good Status Event 1 = Mask VOUT_1.0V Output Power Good Status Event ^[2] |
| 1:0 | RV | 0 | R19 [1:0]: Reserved |

NOTE 1 Not assert GSI_n output signal.

NOTE 2 Not assert GSI_n or POWER_GOOD output signal.

11.4.4 Threshold and Configuration Registers

Table 131 — Register 0x1A

| R1A | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description |
| 7:5 | RW | 110 | R1A [7:5]: VIN_BULK_POWER_GOOD_THRESHOLD_VOLTAGE VIN Bulk Input Threshold Voltage for Input Power Good Status for input supply 000 = Reserved 001 = 9.5 V 010 = 8.5 V 011 = 7.5 V 100 = 6.5 V 101 = 5.5 V 110 = 4.25 V ^{[1],[2],[3]} 111 = Reserved |
| 4 | RV | 0 | R1A [4]: Reserved |
| 3 | RW | 0 | R1A [3]: VBIAS_POWER_GOOD_THRESHOLD_VOLTAGE VBias1 or VBias2 LDO Output (depending on PMIC implementation) Threshold Voltage for Power Good Status 0 = Vendor Specific 1 = Reserved |
| 2 | RW | 0 | R1A [2]: VOUT_1.8V_POWER_GOOD_THRESHOLD_VOLTAGE VOUT 1.8V LDO Output Threshold Voltage for Power Good Status 0 = 1.6 V 1 = Reserved |
| 1 | RW | 0 | R1A [1]: OUTPUT_POWER_SELECT Switch Regulator Output Power Select ^[4] 0 = Report individual power for each rail in R0C, R0D, R0E & R0F or R100, R101, R102, R103, R104, R105, R106, R107 depending on the setting of R32[1:0] 1 = Report total power of each rail in R0C ^[5] or R101+R102 ^[6] |
| 0 | RW | 0 | R1A [0]: VOUT_1.0V_POWER_GOOD_THRESHOLD_VOLTAGE VOUT 1.0V LDO Output Threshold Voltage for Power Good Status 0 = -10% from the setting in Table 148, Register 0x2B [2:1] 1 = -15% from the setting in Table 148, Register 0x2B [2:1] |

NOTE 1 If VIN_Bulk input voltage falls below this threshold, the PMIC may not guarantee the operation.

NOTE 2 If VIN_Bulk voltage continues to fall below vendor specific UVLO, the PMIC triggers an VR Disable command and executes power down sequence.

NOTE 3 If VIN_Bulk voltage threshold is higher than default setting of this register, the PMIC continues to operate but updates its PWR_GOOD status register and GSI_n/PWR_GOOD signal is asserted when VIN_Bulk falls below the threshold setting.

NOTE 4 This register is only applicable if [Table 132, Register 0x1B \[6\]](#) = '1'.

NOTE 5 Host should only read [Table 117, Register 0x0C \[7:0\]](#) for total power if [Table 155, Register 0x32 \[1:0\]](#) = '00'. The register contents of [Table 118, Register 0x0D](#), [Table 119, Register 0x0E](#) and [Table 120, Register 0x0F](#) may not be valid.

NOTE 6 Host should only read [Table 168, Register 0x101 \[2:0\]](#) and [Table 169, Register 0x102 \[7:0\]](#) for total power if [Table 155, Register 0x32 \[1:0\]](#) = '01'. The register contents of [Table 170, Register 0x103](#), [Table 171, Register 0x104](#) and [Table 172, Register 0x105](#), [Table 173, Register 0x106](#), and [Table 174, Register 0x107](#) may not be valid.

11.4.4 Threshold and Configuration Registers (cont'd)

Table 132 — Register 0x1B

| R1B | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description |
| 7 | RW | 0 | R1B [7]: VIN_BULK_OVER_VOLTAGE_THRESHOLD VIN_Bulk Input Over Voltage Threshold Setting 0 = 14.5 V 1 = 16.0 V |
| 6 | RW | 0 | R1B [6]: CURRENT_OR_POWER_METER_SELECT PMIC Output Regulator Measurement - Current or Power Meter ^[1] 0 = Report Current Measurements in registers 1 = Report Power Measurements in registers |
| 5 | RW | 0 | R1B [5]: VIN_MGMT_OVER_VOLTAGE_THRESHOLD VIN_Mgmt Input Over Voltage Threshold 0 = 3.8 V 1 = 3.7 V |
| 4 | RW | 0 | R1B [4]: GLOBAL_PWR_GOOD_PIN_STATUS_MASK Global Mask PWR_GOOD Output Pin ^[2] 0 = Not Masked 1 = Masked |
| 3 | RW | 0 | R1B [3]: GSI_N_PIN_ENABLE Enable GSI_n Pin ^[3] 0 = Disable GSI_n Pin 1 = Enable GSI_n Pin |
| 2:0 | RW | 101 | R1B [2:0]: PMIC_HIGH_TEMPERATURE_WARNING_THRESHOLD PMIC High Temperature Warning Threshold ^[4] 000 = Reserved 001 = PMIC temperature $\geq 85^{\circ}\text{C}$ 010 = PMIC temperature $\geq 95^{\circ}\text{C}$ 011 = PMIC temperature $\geq 105^{\circ}\text{C}$ 100 = PMIC temperature $\geq 115^{\circ}\text{C}$ 101 = PMIC temperature $\geq 125^{\circ}\text{C}$ 110 = PMIC temperature $\geq 135^{\circ}\text{C}$ 111 = Reserved |

- NOTE 1 [Table 117, Register 0x0C \[7:0\]](#) to [Table 120, Register 0x0F \[7:0\]](#) if [Table 155, Register 0x32 \[1:0\]](#) = '00' or [Table 167, Register 0x100 \[7:0\]](#) to [Table 174, Register 0x107 \[7:0\]](#) if [Table 155, Register 0x32 \[1:0\]](#) = '01'.
- NOTE 2 Mask POWER_GOOD output signal for all appropriate register bits in [Table 126, Register 0x15 \[7,5:0\]](#), [Table 127, Register 0x16 \[7:0\]](#), [Table 128, Register 0x17 \[7:4\]](#), [Table 129, Register 0x18 \[7:0\]](#) and [Table 130, Register 0x19 \[4:2\]](#). Mask Register Control [Table 152, Register 0x2F \[1:0\]](#) still applies when Global PWR_GOOD output Mask register is set to '1'.
- NOTE 3 This register can be used as Global Mask Function for GSI_n pin. If disabled, this masks GSI_n output signal for all register bits in [Table 126, Register 0x15 \[7, 5:0\]](#), [Table 127, Register 0x16 \[7:0\]](#), [Table 128, Register 0x17 \[7:2\]](#), [Table 129, Register 0x18 \[7:0\]](#), and [Table 130, Register 0x19 \[4:2\]](#).
- NOTE 4 The tolerance of the temperature warning threshold is $\pm 5^{\circ}\text{C}$ from the selected setting.

11.4.4 Threshold and Configuration Registers (cont'd)

Table 133 — Register 0x1C

| R1C | | | |
|------|-----------|--------------|---|
| Bits | Attribute | Default | Description ^[1] |
| 7:0 | RW | 0011 1100 | <p>R1C [7:0]: SWA_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD SWA Output High Current Consumption Warning Threshold^[2]</p> <p>If Table 155, Register 0x32[1:0] = '00': 0000 0000 = Undefined 0000 0001 \geq 125 mA 0000 0010 \geq 250 mA ... 1111 1111 \geq 31.875 A</p> <p>If Table 155, Register 0x32[1:0] = '01': 0000 0000 = Undefined 0000 0001 \geq 31.25 mA 0000 0010 \geq 62.5 mA ... 1111 1111 \geq 7.968 A</p> |

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 271, Register 0x67](#).

NOTE 2 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [5,0]. For dual phase operation, registers [Table 133, Register 0x1C](#) [7:0] and [Table 134, Register 0x1D](#) [7:0] must be configured identical. For three phase operation, registers [Table 133, Register 0x1C](#) [7:0], [Table 134, Register 0x1D](#) [7:0] and [Table 182, Register 0x11A](#) [7:0] must be configured identical.

11.4.4 Threshold and Configuration Registers (cont'd)

Table 134 — Register 0x1D

| R1D | | | |
|------|-----------|--------------|---|
| Bits | Attribute | Default | Description ^[1] |
| 7:0 | RW | 0011 1100 | <p>R1D [7:0]: SWB_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD SWB Output High Current Consumption Warning Threshold^[2]</p> <p>If Table 155, Register 0x32[1:0] = '00': 0000 0000 = Undefined 0000 0001 \geq 125 mA 0000 0010 \geq 250 mA ... 1111 1111 = $>$ 31.875 A</p> <p>If Table 155, Register 0x32[1:0] = '01': 0000 0000 = Undefined 0000 0001 \geq 31.25 mA 0000 0010 \geq 62.5 mA ... 1111 1111 \geq 7.968 A</p> |

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 272, Register 0x68](#).

NOTE 2 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [5,0]. For dual phase operation, registers [Table 133, Register 0x1C](#) [7:0] and [Table 134, Register 0x1D](#) [7:0] must be configured identical. For three phase operation, registers [Table 133, Register 0x1C](#) [7:0], [Table 134, Register 0x1D](#) [7:0] and [Table 182, Register 0x11A](#) [7:0] must be configured identical.

11.4.4 Threshold and Configuration Registers (cont'd)

Table 135 — Register 0x1E

| R1E | | | |
|------|-----------|--------------|---|
| Bits | Attribute | Default | Description ^[1] |
| 7:0 | RW | 0011 1100 | <p>R1E [7:0]: SWC_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD SWC Output High Current Consumption Warning Threshold^[2]</p> <p>If Table 155, Register 0x32[1:0] = '00': 0000 0000 = Undefined 0000 0001 \geq 125 mA 0000 0010 \geq 250 mA ... 1111 1111 \geq 31.875 A</p> <p>If Table 155, Register 0x32[1:0] = '01': 0000 0000 = Undefined 0000 0001 \geq 31.25 mA 0000 0010 \geq 62.5 mA ... 1111 1111 \geq 7.968 A</p> |

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 273, Register 0x69](#).

NOTE 2 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [6]. For dual phase operation, registers [Table 135, Register 0x1E](#) [7:0] and [Table 183, Register 0x11B](#) [7:0] must be configured identical.

Table 136 — Register 0x1F

| R1F | | | |
|------|-----------|--------------|---|
| Bits | Attribute | Default | Description ^[1] |
| 7:0 | RW | 0010 1000 | <p>R1F [7:0]: SWD_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD SWD Output High Current Consumption Warning Threshold</p> <p>If Table 155, Register 0x32[1:0] = '00': 0000 0000 = Undefined 0000 0001 \geq 125 mA 0000 0010 \geq 250 mA ... 1111 1111 \geq 31.875 A</p> <p>If Table 155, Register 0x32[1:0] = '01': 0000 0000 = Undefined 0000 0001 \geq 31.25 mA 0000 0010 \geq 62.5 mA ... 1111 1111 \geq 7.968 A</p> |

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 274, Register 0x6A](#).

11.4.4 Threshold and Configuration Registers (cont'd)

Table 137 — Register 0x20

| R20 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description ^[1] |
| 7:6 | RW | 01 | R20 [7:6]: SWA_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING COT lvalley_limit 00 = 6A 01 = 7A 10 = 8A 11 = 9A |
| 5:4 | RW | 01 | R20 [5:4]: SWB_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING COT lvalley_limit ^[2] 00 = 6A 01 = 7A 10 = 8A 11 = 9A |
| 3:2 | RW | 01 | R20 [3:2]: SWC_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING COT lvalley_limit ^[3] 00 = 6A 01 = 7A 10 = 8A 11 = 9A |
| 1:0 | RW | 01 | R20 [1:0]: SWD_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING COT lvalley_limit 00 = 4A 01 = 4.5A 10 = 5A 11 = 5.5A |

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 248, Register 0x50](#).

NOTE 2 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [5,0].

NOTE 3 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [6].

11.4.4 Threshold and Configuration Registers (cont'd)

Table 138 — Register 0x21

| R21 | | | |
|------|-----------|----------|---|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7:1 | RW | 011 1100 | R21 [7:1]: SWA_VOLTAGE_SETTING SWA Output Regulator Voltage Setting ^{[3],[4]} 000 0000 = 800 mV ^[5] or 600 mV ^[6] 000 0001 = 805 mV or 605 mV 000 0010 = 810 mV or 610 mV ... 011 1100 = 1100 mV or 900 mV ... 111 1101 = 1425 mV or 1225 mV 111 1110 = 1430 mV or 1230 mV 111 1111 = 1435 mV or 1235 mV |
| 0 | RW | 0 | R21 [0]: SWA_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING SWA Output Threshold Low Side Voltage For Power Good Status 0 = -5% from the setting in Table 138, Register 0x21 [7:1] 1 = -7.5% from the setting in Table 138, Register 0x21 [7:1] |

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 237, Register 0x45](#).

NOTE 2 If required, the host must update the settings in register [Table 138, Register 0x21 \[0\]](#), [Table 139, Register 0x22 \[7:2\]](#) and [Table 137, Register 0x20 \[7:6\]](#) first prior to updating the settings in the register [Table 138, Register 0x21 \[7:1\]](#).

NOTE 3 PMIC guarantees efficiency spec within a range of 1050 mV to 1160 mV.

NOTE 4 After VR is enabled, the host may update this register to any new setting that it may desire. However to prevent false error trigger, the PMIC internally will increment the SWA output voltage setting by 5 mV at a time. The time it takes for PMIC to adjust the output voltage is 5 μ s for each 5 mV increment. The host must wait sufficient time for PMIC to adjust to final value. As an example, if host adjusts the output voltage by 50 mV from the original value, the host must wait minimum of 50 μ s before PMIC can guarantee the new output voltage. During this time, PMIC masks the PWR_GOOD output signal assertion to prevent any artificial error due to the crossing of the output voltage threshold setting. However, PMIC does assert PWR_GOOD output signal if there are any abnormal issues that triggers VR Disable command as described in [Table 27](#). Further, PMIC does monitor PWR_GOOD input signal and executes power off config sequence registers if it is registered low when [Table 155, Register 0x32 \[5\]](#) = '1'.

NOTE 5 [Table 148, Register 0x2B \[5\]](#) = '0'; 5 mV step size.

NOTE 6 [Table 148, Register 0x2B \[5\]](#) = '1'; 5 mV step size

11.4.4 Threshold and Configuration Registers (cont'd)

Table 139 — Register 0x22

| R22 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7:6 | RW | 01 | R22 [7:6]: SWA_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING SWA Output Threshold High Side Voltage For Power Good Status 00 = +5% from the setting in Table 138, Register 0x21 [7:1] 01 = +7.5% from the setting in Table 138, Register 0x21 [7:1] 10 = +10% from the setting in Table 138, Register 0x21 [7:1] 11 = Reserved |
| 5:4 | RW | 10 | R22 [5:4]: SWA_OVER_VOLTAGE_THRESHOLD_SETTING SWA Output Regulator Threshold For Over Voltage Status ^[3] 00 = +7.5% from the setting in Table 138, Register 0x21 [7:1] 01 = +10% from the setting in Table 138, Register 0x21 [7:1] 10 = +12.5% from the setting in Table 138, Register 0x21 [7:1] 11 = Reserved |
| 3:2 | RW | 00 | R22 [3:2]: SWA_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING SWA Output Regulator Threshold For Under Voltage Lockout Status 00 = -10% from the setting in Table 138, Register 0x21 [7:1] 01 = -12.5% from the setting in Table 138, Register 0x21 [7:1] 10 = Reserved 11 = Reserved |
| 1:0 | RW | 00 | R22 [1:0]: SWA_OUTPUT_SOFT_STOP_TIME SWA Output Regulator Soft Stop Time After VR Disable ^[4] 00 = 0.5 ms 01 = 1 ms 10 = 2 ms 11 = 4 ms |

- NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 238, Register 0x46](#).
- NOTE 2 If required, the host must update the setting in register [Table 138, Register 0x21](#) [0], [Table 139, Register 0x22](#) [7:2] and [Table 137, Register 0x20](#) [7:6] first prior to updating the settings in the register [Table 138, Register 0x21](#) [7:1].
- NOTE 3 The setting for the Over Voltage must be higher than Power Good High Side Voltage threshold in [Table 139, Register 0x22](#)[7:6].
- NOTE 4 This is the time it takes for buck regulator to go from steady state voltage to 0 V.

11.4.4 Threshold and Configuration Registers (cont'd)

Table 140 — Register 0x23

| R23 | | | |
|------|-----------|----------|---|
| Bits | Attribute | Default | Description ^{[1],[2],[3]} |
| 7:1 | RW | 011 1100 | R23 [7:1]: SWB_VOLTAGE_SETTING SWB Output Regulator Voltage Setting ^{[4],[5]} 000 0000 = 800 mV ^[6] or 600 mV ^[7] 000 0001 = 805 mV or 605 mV 000 0010 = 810 mV or 610 mV ... 011 1100 = 1100 mV or 900 mV ... 111 1101 = 1425 mV or 1225 mV 111 1110 = 1430 mV or 1230 mV 111 1111 = 1435 mV or 1235 mV |
| 0 | RW | 0 | R23 [0]: SWB_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING SWB Output Threshold Low Side Voltage For Power Good Status 0 = -5% from the setting in Table 140, Register 0x23 [7:1] 1 = -7.5% from the setting in Table 140, Register 0x23 [7:1] |

- NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 239, Register 0x47](#).
- NOTE 2 If required, the host must update the settings in register [Table 140, Register 0x23 \[0\]](#), [Table 141, Register 0x24 \[7:2\]](#) and [Table 137, Register 0x20 \[5:4\]](#) first prior to updating the settings in the register [Table 140, Register 0x23 \[7:1\]](#).
- NOTE 3 This register is only applicable if [Table 247, Register 0x4F \[5,0\]](#) = '00'. For any other setting in [Table 247, Register 0x4F \[5,0\]](#), this register does not apply and it is a don't care.
- NOTE 4 PMIC guarantees efficiency spec within a range of 1050 mV to 1160 mV.
- NOTE 5 After VR is enabled, the host may update this register to any new setting that it may desire. However to prevent false error trigger, the PMIC internally will increment the SWB output voltage setting by 5 mV at a time. The time it takes for PMIC to adjust the output voltage is 5 μ s for each 5 mV increment. The host must wait sufficient time for PMIC to adjust to final value. As an example, if host adjusts the output voltage by 50 mV from the original value, the host must wait minimum of 50 μ s before PMIC can guarantee the new output voltage. During this time, PMIC masks the PWR_GOOD output signal assertion to prevent any artificial error due to the crossing of the output voltage threshold setting. However, PMIC does assert PWR_GOOD output signal if there are any abnormal issues that triggers VR Disable command as described in [Table 27](#). Further, PMIC does monitor PWR_GOOD input signal and executes power off config sequence registers if it is registered low when [Table 155, Register 0x32 \[5\]](#) = '1'.
- NOTE 6 [Table 148, Register 0x2B \[4\]](#) = '0'; 5 mV step size.
- NOTE 7 [Table 148, Register 0x2B \[4\]](#) = '1'; 5 mV step size

11.4.4 Threshold and Configuration Registers (cont'd)

Table 141 — Register 0x24

| R24 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^{[1],[2],[3]} |
| 7:6 | RW | 01 | R24 [7:6]: SWB_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING SWB Output Threshold High Side Voltage For Power Good Status 00 = +5% from the setting in Table 140, Register 0x23 [7:1] 01 = +7.5% from the setting in Table 140, Register 0x23 [7:1] 10 = +10% from the setting in Table 140, Register 0x23 [7:1] 11 = Reserved |
| 5:4 | RW | 10 | R24 [5:4]: SWB_OVER_VOLTAGE_THRESHOLD_SETTING SWB Output Regulator Threshold For Over Voltage Status ^[4] 00 = +7.5% from the setting in Table 140, Register 0x23 [7:1] 01 = +10% from the setting in Table 140, Register 0x23 [7:1] 10 = +12.5% from the setting in Table 140, Register 0x23 [7:1] 11 = Reserved |
| 3:2 | RW | 00 | R24 [3:2]: SWB_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING SWB Output Regulator Threshold For Under Voltage Lockout Status 00 = -10% from the setting in Table 140, Register 0x23 [7:1] 01 = -12.5% from the setting in Table 140, Register 0x23 [7:1] 10 = Reserved 11 = Reserved |
| 1:0 | RW | 00 | R24 [1:0]: SWB_OUTPUT_SOFT_STOP_TIME SWB Output Regulator Soft Stop Time After VR Disable ^[5] 00 = 0.5 ms 01 = 1 ms 10 = 2 ms 11 = 4 ms |

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 240, Register 0x48](#).

NOTE 2 If required, the host must update the settings in register [Table 140, Register 0x23](#) [0], [Table 141, Register 0x24](#) [7:2] and [Table 137, Register 0x20](#) [5:4] first prior to updating the settings in the register [Table 140, Register 0x23](#) [7:1].

NOTE 3 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 4 The setting for the Over Voltage must be higher than Power Good High Side Voltage threshold in [Table 141, Register 0x24](#)[7:6].

NOTE 5 This is the time it takes for buck regulator to go from steady state voltage to 0 V.

11.4.4 Threshold and Configuration Registers (cont'd)

Table 142 — Register 0x25

| R25 | | | |
|------|-----------|----------|--|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7:1 | RW | 011 1100 | R25 [7:1]: SWC_VOLTAGE_SETTING SWC Output Regulator Voltage Setting ^{[3],[4]} 000 0000 = 800 mV ^[5] or 600 mV ^[6] or 400 mV ^[7] 000 0001 = 805 mV or 605 mV or 402.5 mV 000 0010 = 810 mV or 610 mV or 405 mV ... 011 1100 = 1100 mV or 900 mV or 550 mV ... 111 1101 = 1425 mV or 1225 mV or 712.5 mV 111 1110 = 1430 mV or 1230 mV or 715 mV 111 1111 = 1435 mV or 1235 mV or 717.5 mV |
| 0 | RW | 0 | R25 [0]: SWC_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING SWC Output Threshold Low Side Voltage For Power Good Status 0 = -5% from the setting in Table 142, Register 0x25 [7:1] 1 = -7.5% from the setting in Table 142, Register 0x25 [7:1] |

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 241, Register 0x49](#).

NOTE 2 If required, the host must update the settings in register [Table 142, Register 0x25 \[0\]](#), [Table 143, Register 0x26 \[7:2\]](#) and [Table 137, Register 0x20 \[3:2\]](#) first prior to updating the settings in the register [Table 142, Register 0x25 \[7:1\]](#).

NOTE 3 PMIC guarantees efficiency spec within a range of 1050 mV to 1160 mV.

NOTE 4 After VR is enabled, the host may update this register to any new setting that it may desire. However to prevent false error trigger, the PMIC internally will increment the SWC output voltage setting by 5 mV at a time. The time it takes for PMIC to adjust the output voltage is 5 μ s for each 5 mV increment. The host must wait sufficient time for PMIC to adjust to final value. As an example, if host adjusts the output voltage by 50 mV from the original value, the host must wait minimum of 50 μ s before PMIC can guarantee the new output voltage. During this time, PMIC masks the PWR_GOOD output signal assertion to prevent any artificial error due to the crossing of the output voltage threshold setting. However, PMIC does assert PWR_GOOD output signal if there are any abnormal issues that triggers VR Disable command as described in [Table 27](#). Further, PMIC does monitor PWR_GOOD input signal and executes power off config sequence registers if it is registered low when [Table 155, Register 0x32 \[5\]](#) = '1'.

NOTE 5 [Table 184, Register 0x11C \[0\]](#) = '0' and [Table 148, Register 0x2B \[3\]](#) = '0'; 5 mV step size.

NOTE 6 [Table 184, Register 0x11C \[0\]](#) = '0' and [Table 148, Register 0x2B \[3\]](#) = '1'; 5 mV step size

NOTE 7 [Table 184, Register 0x11C \[0\]](#) = '1' and [Table 148, Register 0x2B \[3\]](#) = '0'; 2.5 mV step size.

11.4.4 Threshold and Configuration Registers (cont'd)

Table 143 — Register 0x26

| R26 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7:6 | RW | 01 | R26 [7:6]: SWC_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING SWC Output Threshold High Side Voltage For Power Good Status 00 = +5% from the setting in Table 142, Register 0x25 [7:1] 01 = +7.5% from the setting in Table 142, Register 0x25 [7:1] 10 = +10% from the setting in Table 142, Register 0x25 [7:1] 11 = Reserved |
| 5:4 | RW | 10 | R26 [5:4]: SWC_OVER_VOLTAGE_THRESHOLD_SETTING SWC Output Regulator Threshold For Over Voltage Status ^[3] 00 = +7.5% from the setting in Table 142, Register 0x25 [7:1] 01 = +10% from the setting in Table 142, Register 0x25 [7:1] 10 = +12.5% from the setting in Table 142, Register 0x25 [7:1] 11 = Reserved |
| 3:2 | RW | 00 | R26 [3:2]: SWC_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING SWC Output Regulator Threshold For Under Voltage Lockout Status 00 = -10% from the setting in Table 142, Register 0x25 [7:1] 01 = -12.5% from the setting in Table 142, Register 0x25 [7:1] 10 = Reserved 11 = Reserved |
| 1:0 | RW | 00 | R26 [1:0]: SWC_OUTPUT_SOFT_STOP_TIME SWC Output Regulator Soft Stop Time After VR Disable ^[4] 00 = 0.5 ms 01 = 1 ms 10 = 2 ms 11 = 4 ms |

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 242, Register 0x4A](#).

NOTE 2 If required, the host must update the settings in register [Table 142, Register 0x25](#) [0], [Table 143, Register 0x26](#) [7:2] and [Table 137, Register 0x20](#) [3:2] first prior to updating the settings in the register [Table 142, Register 0x25](#) [7:1].

NOTE 3 The setting for the Over Voltage must be higher than Power Good High Side Voltage threshold in [Table 143, Register 0x26](#)[7:6].

NOTE 4 This is the time it takes for buck regulator to go from steady state voltage to 0 V.

11.4.4 Threshold and Configuration Registers (cont'd)

Table 144 — Register 0x27

| R27 | | | |
|------|-----------|----------|--|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7:1 | RW | 011 1100 | R27 [7:1]: SWD_VOLTAGE_SETTING SWD Output Regulator Voltage Setting ^{[3],[4]} 000 0000 = 1500 mV ^[5] or 2200 mV ^[6] 000 0001 = 1505 mV or 2205 mV 000 0010 = 1510 mV or 2210 mV ... 011 1100 = 1800 mV or 2500 mV ... 111 1101 = 2125 mV or 2825 mV 111 1110 = 2130 mV or 2830 mV 111 1111 = 2135 mV or 2835 mV |
| 0 | RW | 0 | R27 [0]: SWD_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING SWD Output Threshold Low Side Voltage For Power Good Status 0 = -5% from the setting in Table 144, Register 0x27 [7:1] 1 = -7.5% from the setting in Table 144, Register 0x27 [7:1] |

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 243, Register 0x4B](#).

NOTE 2 If required, the host must update the settings in register [Table 144, Register 0x27 \[0\]](#), [Table 145, Register 0x28 \[7:2\]](#) and [Table 137, Register 0x20 \[1:0\]](#) first prior to updating the settings in the register [Table 144, Register 0x27 \[7:1\]](#).

NOTE 3 PMIC guarantees efficiency spec within a range of 1750 mV to 1850 mV.

NOTE 4 After VR is enabled, the host may update this register to any new setting that it may desire. However to prevent false error trigger, the PMIC internally will increment the SWD output voltage setting by 5 mV at a time. The time it takes for PMIC to adjust the output voltage is 5 μ s for each 5 mV increment. The host must wait sufficient time for PMIC to adjust to final value. As an example, if host adjusts the output voltage by 50 mV from the original value, the host must wait minimum of 50 μ s before PMIC can guarantee the new output voltage. During this time, PMIC masks the PWR_GOOD output signal assertion to prevent any artificial error due to the crossing of the output voltage threshold setting. However, PMIC does assert PWR_GOOD output signal if there are any abnormal issues that triggers VR Disable command as described in [Table 27](#). Further, PMIC does monitor PWR_GOOD input signal and executes power off config sequence registers if it is registered low when [Table 155, Register 0x32 \[5\]](#) = '1'.

NOTE 5 [Table 148, Register 0x2B \[0\]](#) = '0'; 5 mV step size.

NOTE 6 [Table 148, Register 0x2B \[0\]](#) = '1'; 5 mV step size.

11.4.4 Threshold and Configuration Registers (cont'd)

Table 145 — Register 0x28

| R28 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7:6 | RW | 01 | R28 [7:6]: SWD_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING SWD Output Threshold High Side Voltage For Power Good Status 00 = +5% from the setting in Table 144, Register 0x27 [7:1] 01 = +7.5% from the setting in Table 144, Register 0x27 [7:1] 10 = +10% from the setting in Table 144, Register 0x27 [7:1] 11 = Reserved |
| 5:4 | RW | 10 | R28 [5:4]: SWD_OVER_VOLTAGE_THRESHOLD_SETTING SWD Output Regulator Threshold For Over Voltage Status ^[3] 00 = +7.5% from the setting in Table 144, Register 0x27 [7:1] 01 = +10% from the setting in Table 144, Register 0x27 [7:1] 10 = +12.5% from the setting in Table 144, Register 0x27 [7:1] 11 = Reserved |
| 3:2 | RW | 00 | R28 [3:2]: SWD_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING SWD Output Regulator Threshold For Under Voltage Lockout Status 00 = -10% from the setting in Table 144, Register 0x27 [7:1] 01 = -12.5% from the setting in Table 144, Register 0x27 [7:1] 10 = Reserved 11 = Reserved |
| 1:0 | RW | 00 | R28 [1:0]: SWD_OUTPUT_SOFT_STOP_TIME SWD Output Regulator Soft Stop Time After VR Disable ^[4] 00 = 1 ms 01 = 2 ms 10 = 4 ms 11 = 8 ms |

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 244, Register 0x4C](#).

NOTE 2 If required, the host must update the settings in register [Table 144, Register 0x27](#) [0], [Table 145, Register 0x28](#) [7:2] and [Table 137, Register 0x20](#) [1:0] first prior to updating the settings in the register [Table 144, Register 0x27](#) [7:1].

NOTE 3 The setting for the Over Voltage must be higher than Power Good High Side Voltage threshold in [Table 145, Register 0x28](#)[7:6].

NOTE 4 This is the time it takes for buck regulator to go from steady state voltage to 0 V.

11.4.4 Threshold and Configuration Registers (cont'd)

Table 146 — Register 0x29

| R29 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7:6 | RW | 10 | R29 [7:6]: SWA_MODE_SELECT SWA Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode) |
| 5:4 | RW | 01 | R29 [5:4]: SWA_SWITCHING_FREQ SWA Output Regulator Switching Frequency 00 = 500 KHz 01 = 750 KHz 10 = Reserved 11 = Reserved |
| 3:2 | RW | 10 | R29 [1:0]: SWB_MODE_SELECT SWB Output Regulator Mode Selection ^[3] 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode) |
| 1:0 | RW | 01 | R29 [1:0]: SWB_SWITCHING_FREQ SWB Output Regulator Switching Frequency ^[3] 00 = 500 KHz 01 = 750 KHz 10 = Reserved 11 = Reserved |

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 245, Register 0x4D](#).

NOTE 2 If required, the host must adjust this register first before issuing VR Enable command in [Table 155, Register 0x32](#) [7].

NOTE 3 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

11.4.4 Threshold and Configuration Registers (cont'd)

Table 147 — Register 0x2A

| R2A | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7:6 | RW | 10 | R2A [7:6]: SWC_MODE_SELECT Switch Node C Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode) |
| 5:4 | RW | 01 | R2A [5:4]: SWC_SWITCHING_FREQ Switch Node C Output Regulator Switching Frequency ^[3] 00 = 500 KHz 01 = 750 KHz 10 = Reserved 11 = Reserved |
| 3:2 | RW | 10 | R2A [3:2]: SWD_MODE_SELECT Switch Node D Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode) |
| 1:0 | RW | 01 | R2A [1:0]: SWD_SWITCHING_FREQ Switch Node D Output Regulator Switching Frequency 00 = Reserved 01 = 750 KHz 10 = 1000 KHz 11 = Reserved |

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 246, Register 0x4E](#).

NOTE 2 If required, the host must adjust this register first before issuing VR Enable command in [Table 155, Register 0x32 \[7\]](#).

11.4.4 Threshold and Configuration Registers (cont'd)

Table 148 — Register 0x2B

| R2B | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7:6 | RW | 01 | R2B [7:6]: VOUT_1.8V_VOLTAGE_SETTING VOUT 1.8 V LDO Output Voltage Setting ^[3] 00 = 1.7 V 01 = 1.8 V 10 = 1.9 V 11 = Reserved |
| 5 | RW | 0 | R2B [5]: SWA_VOLTAGE_RANGE SWA Output Voltage Range Selection ^[4] 0 = Range: 800 mV to 1435 mV for SWA; 5 mV step size 1 = Range: 600 mV to 1235 mV for SWA; 5 mV step size |
| 4 | RW | 0 | R2B [4]: SWB_VOLTAGE_RANGE SWB Output Voltage Range Selection ^{[5],[6]} 0 = Range: 800 mV to 1435 mV for SWB; 5 mV step size 1 = Range: 600 mV to 1235 mV for SWB; 5 mV step size |
| 3 | RW | 0 | R2B [3]: SWC_VOLTAGE_RANGE SWC Output Voltage Range Selection ^[7] . The MSB bit Table 184, Register 0x11C [0] plus this LSB bit Table 148, Register 0x2B [3] makes 2 bit encoding as following: 00 = Range: 800 mV to 1435 mV for SWC; 5 mV step size 01 = Range: 600 mV to 1235 mV for SWC; 5 mV step size 10 = Range: 400 mV to 717.5 mV for SWC; 2.5 mV step size 11 = Reserved |
| 2:1 | RW | 01 | R2B [2:1]: VOUT_1.0V_VOLTAGE_SETTING VOUT 1.0 V LDO Voltage Setting ^[8] 00 = 0.9 V 01 = 1.0 V 10 = 1.1 V 11 = 1.2 V |
| 0 | RW | 0 | R2B [0]: SWD_VOLTAGE_RANGE SWD Output Voltage Range Selection ^[9] 0 = Range: 1500 mV to 2135 mV for SWD; 5 mV step size 1 = Range: 2200 mV to 2835 mV for SWD; 5 mV step size |

- NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 249, Register 0x51](#).
- NOTE 2 If required, the host must adjust this register first before issuing VR Enable command in [Table 155, Register 0x32](#) [7]. The host must also wait minimum of 5 μ s after the adjustment before issuing VR Enable command.
- NOTE 3 The VOUT_1.8V Power Good threshold in register [Table 131, Register 0x1A](#) [2] is always fixed regardless of the setting in this register.
- NOTE 4 Range and resolution selection applies to register [Table 138, Register 0x21](#) [7:1].
- NOTE 5 Range and resolution selection applies to register [Table 140, Register 0x23](#) [7:1].
- NOTE 6 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.
- NOTE 7 Range selection applies to registers [Table 142, Register 0x25](#) [7:1].
- NOTE 8 If required, the host must adjust this register one step at a time (0.1 V increment or decrement) to prevent false trigger of power good status and PWR_GOOD pin assertion. In other words, host should not increment or decrement 0.2 V or 0.3 V from its current setting.
- NOTE 9 Range and resolution selection applies to register [Table 144, Register 0x27](#) [7:1].

11.4.4 Threshold and Configuration Registers (cont'd)

Table 149 — Register 0x2C

| R2C | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7:5 | RW | 001 | R2C [7:5]: SWA_OUTPUT_SOFT_START_TIME SWA Output Regulator Soft Start Time After VR Enable ^[3] 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms ... 111 = 14 ms |
| 4 | RV | 0 | R2C [4]: Reserved |
| 3:1 | RW | 001 | R2C [3:1]: SWB_OUTPUT_SOFT_START_TIME SWB Output Regulator Soft Start Time After VR Enable ^{[3],[4]} 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms ... 111 = 14 ms |
| 0 | RV | 0 | R2C [0]: Reserved |

- NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 261, Register 0x5D](#).
- NOTE 2 If required, the host must adjust this register first before issuing VR Enable command in [Table 155, Register 0x32 \[7\]](#).
- NOTE 3 This is the time it takes for buck regulator to go from 0 V to steady state voltage (the actual voltage varies based on pre-programmed voltage).
- NOTE 4 This register is only applicable if [Table 247, Register 0x4F \[5,0\]](#) = '00'. For any other setting in [Table 247, Register 0x4F \[5,0\]](#), this register does not apply and it is a don't care.

11.4.4 Threshold and Configuration Registers (cont'd)

Table 150 — Register 0x2D

| R2D | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7:5 | RW | 001 | R2D [7:5]: SWC_OUTPUT_SOFT_START_TIME SWC Output Regulator Soft Start Time After VR Enable ^[3] 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms ... 111 = 14 ms |
| 4 | RV | 0 | R2D [4]: Reserved |
| 3:1 | RW | 001 | R2D [3:1]: SWD_OUTPUT_SOFT_START_TIME SWD Output Regulator Soft Start Time After VR Enable ³ 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms ... 111 = 14 ms |
| 0 | RV | 0 | R2D [0]: Reserved |

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 262, Register 0x5E](#).

NOTE 2 If required, the host must adjust this register first before issuing VR Enable command in [Table 155, Register 0x32](#) [7].

NOTE 3 This is the time it takes for buck regulator to go from 0 V to steady state voltage (the actual voltage varies based on pre-programmed voltage)

Table 151 — Register 0x2E

| R2E | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description |
| 7:3 | RV | 0 | R2E [7:3]: Reserved |
| 2:0 | RW | 100 | R2E [2:0]: PMIC_SHUTDOWN_TEMPERATURE_THRESHOLD PMIC Shutdown Temperature Threshold 000 = PMIC Temperature $\geq 105^{\circ}\text{C}$ 001 = PMIC Temperature $\geq 115^{\circ}\text{C}$ 010 = PMIC Temperature $\geq 125^{\circ}\text{C}$ 011 = PMIC Temperature $\geq 135^{\circ}\text{C}$ 100 = PMIC Temperature $\geq 145^{\circ}\text{C}$ 101 = Reserved 110 = Reserved 111 = Reserved |

11.4.4 Threshold and Configuration Registers (cont'd)

Table 152 — Register 0x2F

| Bits | R2F | | |
|------|-----------|---------|--|
| | Attribute | Default | Description |
| 7 | RW | 0 | R2F [7]: VIN_MGMT_INPUT_SUPPLY_SWITCHOVER_THRESHOLD VIN_Mgmt Input Supply Switchover Voltage Threshold to VIN_Bulk Input Supply 0 = Vendor Specific ^[1] 1 = Reserved |
| 6 | RW | 0 | R2F [6]: SWA_REGULATOR_CONTROL Disable SWA Regulator Output ^{[2],[3]} 0 = Disable Switch Node A Output Regulator 1 = Enable Switch Node A Output Regulator |
| 5 | RW | 0 | R2F [5]: SWB_REGULATOR_CONTROL Disable SWB Regulator Output ^{[2],[3],[4]} 0 = Disable Switch Node B Output Regulator 1 = Enable Switch Node B Output Regulator |
| 4 | RW | 0 | R2F [4]: SWC_REGULATOR_CONTROL Disable SWC Regulator Output ^{[2],[3]} 0 = Disable Switch Node C Output Regulator 1 = Enable Switch Node C Output Regulator |
| 3 | RW | 0 | R2F [3]: SWD_REGULATOR_CONTROL Disable SWD Regulator Output ^{[2],[3]} 0 = Disable Switch Node D Output Regulator 1 = Enable Switch Node D Output Regulator |
| 2 | RW | 0 | R2F [2]: WRITE_PROTECT_FUNCTION_CONTROL PMIC write-protect Function Control ^[5] 0 = CAMP input signal determines the write-protect Function as noted in clause 6.9.1 1 = Write-protect Function is disabled; All register write access is allowed independent of CAMP input signal as noted in clause 6.9.1. |
| 1:0 | RW | 10 | R2F [1:0]: MASK_BITS_REGISTER_CONTROL Mask Bits Register Control ^[6] 00 = Mask GSI_n Signal Only (PWR_GOOD Signal will assert) 01 = Mask PWR_GOOD Signal Only (GSI_n Signal will assert) 10 = Mask GSI_n and PWR_GOOD Signals (neither PWR_GOOD assert or GSI_n signal will assert) 11 = Reserved |

NOTE 1 The VIN_Mgmt input switchover voltage threshold range is vendor specific and can vary between 2.6 V to 2.9 V max.

- NOTE 2 This bit must be used only after power up sequence (after VR Enable command). At first power up, PMIC automatically updates the status of this register to '1' after VR Enable command. When VR Enable command is registered, the PMIC updates this register based on Power On Sequence Configuration (0 to 5) setting. If enabled in Power On Sequence Configuration 0 to 5 registers, only then, under non write-protect mode of operation, the PMIC's output regulator can be disabled by clearing this bit and they can be re-enabled again by setting this bit. The PMIC does not alter its Power Good output signal and keeps it asserted High. If any regulator is not enabled in Power on Sequence Configuration 0 to 5, it cannot be enabled using this register. For example, if only SWA is enabled and SWB, SWC, SWD, SWE and SWF are not enabled in [Table 232, Register 0x40 \[7:0\]](#) to [Table 236, Register 0x44 \[7:0\]](#), [Table 265, Register 0x61 \[7:0\]](#) then only SWA can be disabled and then re-enabled again but SWB, SWC, SWD, SWE and SWF cannot be enabled using [Table 152, Register 0x2F \[6:3\]](#), [Table 191, Register 0x123 \[1:0\]](#).
- NOTE 3 In non write-protect mode, after VR enable command, if any output regulators are disabled by clearing [Table 152, Register 0x2F \[6:3\]](#), [Table 191, Register 0x123 \[1:0\]](#) and then if host issues VR Disable command or PMIC internally triggers VR Disable command, the PMIC keeps the disabled output regulator in [Table 152, Register 0x2F \[6:3\]](#), [Table 191, Register 0x123 \[1:0\]](#) off and remaining output regulators are disabled by following the Power Off Sequence Configuration 0 to 5 settings.
- NOTE 4 This register is only applicable if [Table 247, Register 0x4F \[5,0\]](#) = '00'. For any other setting in [Table 247, Register 0x4F \[5,0\]](#), this register does not apply and it is a don't care.
- NOTE 5 At first power on, this register is automatically configured identically by the PMIC on its own as [Table 263, Register 0x5F \[7\]](#).
- NOTE 6 Applies to Mask Registers [Table 126, Register 0x15 \[7,5:0\]](#), [Table 127, Register 0x16 \[7:0\]](#), [Table 128, Register 0x17 \[7:2\]](#), [Table 129, Register 0x18 \[7:0\]](#), [Table 130, Register 0x19 \[4:2\]](#), [Table 180, Register 0x114 \[7:0\]](#) and [Table 181, Register 0x115 \[7:6\]](#). when any one or more Mask registers are set to '1'. If all Mask registers are configured as '0', the setting in this register ([Table 152, Register 0x2F \[1:0\]](#)) does not matter.

11.4.4 Threshold and Configuration Registers (cont'd)

Table 153 — Register 0x30

| R30 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description |
| 7 | RW | 0 | R30 [7]: ADC_ENABLE Enable ADC (Analog to Digital Conversion) 0 = Disable ^[1] 1 = Enable |
| 6:3 | RW | 0 | R30 [6:3]: ADC_SELECT Input Selection for ADC Readout ^[2] 0000 = SWA Output Voltage 0001 = SWB Output Voltage ^[3] 0010 = SWC Output Voltage 0011 = SWD Output Voltage 0100 = SWE Output Voltage ^[3] 0101 = VIN_Bulk Input Voltage 0110 = VIN_Mgmt Input Voltage 0111 = VBIAS1 Output Voltage ^[4] 1000 = VOUT_1.8V Output Voltage 1001 = VOUT_1.0V Output Voltage 1010 = SWF Output Voltage ^[5] 1011 = VBIAS2 Output Voltage ^[4] All other encodings are reserved. |
| 2 | RW | 0 | R30 [2]: REGISTER_ADDRESSING_MODE Register Addressing for I ² C and I ³ C Protocol ^[6] 0 = 1 Byte address; Configuration register space is limited to first 256 Bytes 1 = 2 Byte address; Configuration register space is up to 64K Bytes |
| 1:0 | RW | 0 | R30 [1:0]: ADC_REGISTER_UPDATE_FREQUENCY ADC Current or Power Measurement Update Frequency ^{[7],[8]} 00 = 1 ms 01 = 2 ms 10 = 4 ms 11 = 8 ms |

- NOTE 1 Disables the ADC function completely. Applies to voltage readout in [Table 154, Register 0x31 \[7:0\]](#) as well as current or power readout in [Table 117, Register 0x0C \[7:0\]](#), [Table 118, Register 0x0D \[5:0\]](#), [Table 119, Register 0x0E \[5:0\]](#) and [Table 120, Register 0x0F \[5:0\]](#). Does not apply to thermal sensor temperature readout in [Table 157, Register 0x33 \[7:5\]](#) as well as high temperature warning and critical temperature shutdown.
- NOTE 2 The host shall wait minimum of 9 ms delay after the input selection for ADC readout and the actual readout from [Table 154, Register 0x31](#) to get the latest reading
- NOTE 3 Only applicable if [Table 247, Register 0x4F \[5,0\]](#) = '00'. For any other setting in [Table 247, Register 0x4F \[5,0\]](#), this encoding does not apply and it is a don't care.
- NOTE 4 PMIC may implement only one VBIAS LDO output regulator or two VBIAS LDO output regulators. If only one VBIAS LDO output regulator is used, VBIAS1 code (0111) should be used to read out the output LDO voltage status. If two VBIAS LDO output regulators are used, both VBIAS1 (0111) and VBIAS2 (1011) can be used to read out the output LDO voltage status individually.
- NOTE 5 Only applicable if [Table 247, Register 0x4F \[6\]](#) = '0'. For any other setting in [Table 247, Register 0x4F \[6\]](#), this encoding does not apply and it is a don't care.
- NOTE 6 When there is a change in addressing mode, STOP operation is required on I²C or I³C bus.
- NOTE 7 For average output current or power measurement in registers [Table 117, Register 0x0C \[7:0\]](#) to [Table 120, Register 0x0F \[7:0\]](#) or [Table 167, Register 0x100 \[7:0\]](#) to [Table 174, Register 0x107 \[7:0\]](#).
- NOTE 8 This register represents how often the registers are updated. The internal sampling rate is vendor specific.

11.4.4 Threshold and Configuration Registers (cont'd)

Table 154 — Register 0x31

| R31 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description |
| 7:0 | RO | 0 | <p>R31 [7:0]: ADC_READ</p> <p>ADC Output Voltage Reading^[1](Applies to SW[A:F], VOUT_1.8V, VOUT_1.0V, VIN_Mgmt)</p> <p>0000 0000 = Undefined</p> <p>0000 0001 = 15 mV</p> <p>0000 0010 = 30 mV</p> <p>..</p> <p>1111 1111 > = 3825 mV</p> <p>ADC Output Voltage Reading^[2] (Applies to VIN_Bulk Input Voltage)</p> <p>0000 0000 = Undefined</p> <p>0000 0001 = 70 mV</p> <p>0000 0010 = 140 mV</p> <p>..</p> <p>1111 1111 > = 17850 mV</p> <p>ADC Output Voltage Reading^[3] (Applies to VBias1 or VBias2 Output Voltage)</p> <p>0000 0000 = Undefined</p> <p>0000 0001 = 25 mV</p> <p>0000 0010 = 50 mV</p> <p>..</p> <p>1111 1111 > = 6375 mV</p> |

NOTE 1 Only valid when [Table 153, Register 0x30](#) [6:3] = '0000' or '0001' or '0010' or '0011' or '0100' or '1010' or '0110' or '1000' or '1001'.

NOTE 2 Only valid when [Table 153, Register 0x30](#) [6:3] = '0101'.

NOTE 3 Only valid when [Table 153, Register 0x30](#) [6:3] = '0111' or '1011'.

11.4.4 Threshold and Configuration Registers (cont'd)

Table 155 — Register 0x32

| R32 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description |
| 7 | RW | 0 | R32 [7]: VR_ENABLE PMIC Enable ^{[1],[2],[3],[4],[5],[6]} 0 = PMIC Disable 1 = PMIC Enable |
| 6 | RO | 0 | R32 [6]: MANAGEMENT_INTERFACE_SELECTION PMIC Management Bus Interface Protocol Selection ^[7] 0 = I ² C Protocol (Max speed 1 MHz) 1 = I3C Basic Protocol |
| 5 | RW | 1 | R32 [5]: EXECUTE_VR_ENABLE_CONTROL PMIC VR Enable Command Execution Control over I ² C/I3C Bus or VR_OE or Auto Power On ^{[4],[5],[6]} 0 = Do Not Execute VR Enable Command; i.e., ignore bit [7] = '1' and keep it as '0'. 1 = Execute VR Enable Command |
| 4 | RW | 0 | R32 [4]: EXECUTE_CAMP_FAIL_N_FUNCTION_CONTROL PMIC CAMP Fail_n function (Transition from High to Low) Control ^[8] 0 = Execute VR Disable Command 1 = Do Not Execute VR Disable Command |
| 3 | RW | 0 | R32 [3]: CAMP_PWR_GOOD_OUTPUT_SIGNAL_CONTROL PMIC CAMP PWR_GOOD Output Signal Control 0 = PMIC controls PWR_GOOD output on its own based on internal status 1 = PWR_GOOD Output Float ^[9] |
| 2 | RV | 0 | R32 [2]: Reserved |
| 1:0 | RW | 00 | R32 [1:0]: ADC_ACCURACY_STEP_SIZE ADC Accuracy Step Size ^[10] 00 = 125 mA or 125 mW ^[11] 01 = 31.25 mA or 31.25 mW ^[12] All other encodings are reserved |

NOTE 1 The PMIC updates this bit when VR_OE signal transitions to high or when host issues VR Enable command over I²C/I3C Basic Bus; whichever comes first. PMIC also updates this bit when VR_OE signal transitions to low or when host issues VR Disable command over I²C/I3C Basic bus in programmable mode; whichever comes first. Further, PMIC updates this bit when CAMP input is low (if [Table 155, Register 0x32](#) [4] = '0') or when PMIC internally generates VR Disable command due to fault condition regardless of PMIC's VR_OE signal.

NOTE 2 Host sets this bit at first power on. After this bit is set, the PMIC executes Power On Sequence configuration 0 ([Table 232, Register 0x40](#)) to Power On Sequence configuration 4 ([Table 236, Register 0x44](#)) and Power On Sequence configuration 5 ([Table 265, Register 0x61](#)) registers.

NOTE 3 The host shall ensure that prior to issuing VR Enable command, there is no pending IBI interrupt (i.e., [Table 115, Register 0x0A](#) [1] = '1') status. After host issues VR Enable command, the PMIC may NACK any I²C or I3C Basic bus transaction by host until tPMIC_PWR_GOOD_OUT timing parameter is satisfied. The host shall not access any device specific registers or issue any CCCs until tPMIC_PWR_GOOD_OUT parameter is satisfied. The PMIC device may request for an IBI during power up sequence (i.e., during tPMIC_PWR_GOOD_OUT time) if there is any event.

NOTE 4 After host issues VR Enable command, the PMIC may NACK any I2C or I3C Basic bus transactions by host until tPMIC_PWR_GOOD_OUT timing parameter is satisfied.

- NOTE 5 Once [Table 155, Register 0x32](#) [7] is set to '1' via VR Enable command, the subsequent write to register [Table 155, Register 0x32](#) [5] = '0' is ignored by the PMIC. If there is a simultaneous write to register [Table 155, Register 0x32](#) [7,5] = '10', the PMIC prioritizes bit [5] and does not execute VR Enable command.
- NOTE 6 See [Table 156](#).
- NOTE 7 This register is automatically updated when SETAASA CCC or RSTDAA CCC is registered by the PMIC device or when PMIC device goes through bus reset as described in clause 7.8 regardless of whether PMIC is in write-protect mode or non write-protect mode of operation. This register can be read by the Host through normal Read operation but it cannot be written with normal write operation either in I²C mode or I3C Basic mode of operation. When this register is updated, it takes in effect where there is a next START operation (i.e., after STOP operation).
- NOTE 8 At first power on, this register is automatically configured identically by the PMIC on its own as [Table 263, Register 0x5F](#) [4].
- NOTE 9 When this encoding is set, the PMIC always floats the PWR_GOOD output signal even when there is an internal VR Disable command due to fault condition.
- NOTE 10 When Host changes ADC accuracy step size, it should also update the threshold setting in [Table 133, Register 0x1C](#) to [Table 136, Register 0x1F](#), [Table 182, Register 0x11A](#), [Table 183, Register 0x11B](#).
- NOTE 11 With the coarse ADC accuracy, the register readout is in [Table 117, Register 0x0C](#) to [Table 120, Register 0x0F](#) and register threshold setting in [Table 133, Register 0x1C](#) to [Table 136, Register 0x1F](#) is limited to 31.875A.
- NOTE 12 With the granular ADC accuracy, the register readout is in [Table 167, Register 0x100](#) to [Table 174, Register 0x107](#) is limited to 31.968A; the register threshold setting in [Table 133, Register 0x1C](#) to [Table 136, Register 0x1F](#) and [Table 182, Register 0x11A](#), [Table 183, Register 0x11B](#) is limited to 7.968A.

Table 156 — PMIC Action for Register R32[7,5] Setting

| R32[7,5] | If Output Regulators are On | If Output Regulators are Off |
|----------|----------------------------------|------------------------------|
| 00 | Execute VR Disable | No Action |
| 01 | Execute VR Disable | No Action |
| 10 | No Action; Regulators remains On | Regulators remains Off |
| 11 | No Action | Execute VR Enable |

11.4.4 Threshold and Configuration Registers (cont'd)

Table 157 — Register 0x33

| R33 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description |
| 7:5 | RO | 0 | R33 [7:5]: TEMPERATURE_MEASUREMENT PMIC Temperature ^[1] 000 = $\leq 85^{\circ}\text{C}$ 001 = 85°C 010 = 95°C 011 = 105°C 100 = 115°C 101 = 125°C 110 = 135°C 111 = $> 140^{\circ}\text{C}$ |
| 4 | RO | 0 | R33 [4]: VIN_MGMT_POWER_GOOD_STATUS_SWITCHOVER_MODE VIN_Mgmt Input Supply Power Good Status in Switchover Mode Only ^[2] 0 = Power Not Good 1 = Power Good |
| 3 | RO | 0 | R33 [3]: VBIAS_OR_VIN_BULK_UNDER_VOLTAGE_LOCKOUT_STATUS VBias or VIN_Bulk Under Voltage Lockout Status ^[3] 0 = No Under Voltage Lockout 1 = Under Voltage Lockout |
| 2 | RO | 0 | R33 [2]: VOUT_1.0V_OUTPUT_POWER_GOOD_STATUS VOUT_1.0V LDO Output Power Good Status ^[4] 0 = Power Good 1 = Power Not Good |
| 1:0 | RV | 0 | R33 [1:0]: Reserved |

NOTE 1 The accuracy of the temperature readout code is $\pm 5^{\circ}\text{C}$.

NOTE 2 This register has no meaning when PMIC is NOT in switchover mode. In switchover mode only, when PMIC detects VIN_Mgmt input supply from the platform, this bit is set to indicate that PMIC now recognizes valid VIN_Mgmt input power supply.

NOTE 3 This register is set when either VBias1 or VBias2 LDO output (depending on PMIC implementation) goes below vendor specific threshold or VIN_Bulk input goes below vendor specific threshold.

NOTE 4 This register is set when VOUT_1.0V output drops below the threshold setting in register [Table 131, Register 0x1A](#) [0].

11.4.4 Threshold and Configuration Registers (cont'd)

Table 158 — Register 0x34

| R34 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description ^[1] |
| 7 | RO | 0 | R34 [7]: PEC_ENABLE Packet Error Code Enable ^[2] (Applicable Only if R32 [6] = '1') 0 = Disable 1 = Enable |
| 6 | RO | 0 | R34 [6]: IBI_ENABLE In Band Interrupt Enable ^[3] (Applicable Only if R32 [6] = '1') 0 = Disable 1 = Enable |
| 5 | RO | 0 | R34 [5]: PARITY_DISABLE T Bit Parity Code Disable ² (Applicable Only if R32 [6] = '1'.) 0 = Enable 1 = Disable ^[4] |
| 4 | RV | 0 | R34 [4]: Reserved |
| 3:1 | RO | 111 | R34 [3:1]: HID_CODE PMIC's 3-bit HID Code ^[5] 000 001 010 011 100 101 110 111 |
| 0 | RV | 0 | R34 [0]: Reserved |

NOTE 1 The write (or update) transaction to this register must be followed by STOP operation to allow the PMIC device to update the setting.

NOTE 2 This register is automatically updated when RSTDAA CCC is registered by the PMIC device or when PMIC device goes through bus reset as described in clause 7.7. This register cannot be written by the Host through normal write operation either in I²C mode or I3C mode of operation. This register is updated with DEVCTRL CCC with RegMod='0' only. This register cannot be written with DEVCTRL CCC with RegMod='1'.

NOTE 3 This register is automatically updated when ENEC CCC or DISEC CCC or RSTDAA CCC is registered by the PMIC device or when PMIC device goes through bus reset as described in clause 7.7. This register can be read by the Host through normal Read operation but it cannot be written with normal write operation either in I²C mode or I3C mode of operation. This register cannot be written with DEVCTRL CCC with RegMod='1'.

NOTE 4 When Parity function is disabled, the PMIC simply ignores the "T" bit information from the Host. The host may actually choose to compute the parity and send that information in "T" bit or simply drive static low or high in "T" bit.

NOTE 5 This register is updated when PMIC device receives SETHID CCC or when PMIC device goes through bus reset as described in clause 7.7. This register cannot be written with DEVCTRL CCC with RegMod='1'.

11.4.4 Threshold and Configuration Registers (cont'd)

Table 159 — Register 0x35

| R35 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^{[1],[2],[3]} |
| 7 | RW | 0 | R35 [7]: ERROR_INJECTION_ENABLE Error Injection Enable ^[4] 0 = Disable 1 = Enable |
| 6:4 | RW | 0 | R35 [6:4]: ERROR_INJECTION_RAIL_SELECTION Error Injection - Input Rail and Output Rail Selection ^{[5],[6]} 000 = Undefined 001 = SWA Output Only 010 = SWB Output Only 011 = SWC Output Only 100 = SWD Output Only 101 = VIN_Bulk Input Only 110 = VIN_Mgmt Input Only 111 = Do Not Use |
| 3 | RW | 0 | R35 [3]: OVER_VOLTAGE_UNDER_VOLTAGE_SELECT Over Voltage or Under Voltage Selection for Bits [6:4] ^[7] 0 = Over Voltage 1 = Under Voltage ^[8] |
| 2:0 | RW | 0 | R35[2:0]: MISC_ERROR_INJECTION_TYPE Miscellaneous Error Injection Type ^[9] 000 = Undefined 001 = VIN_Mgmt to VIN_Bulk Switchover 010 = Critical Temperature Shutdown 011 = High Temperature Warning Threshold 100 = VOUT_1.8V LDO Power Good 101 = High Current Consumption Warning ^[10] 110 = Reserved 111 = Current Limiter Warning ^[10] |

- NOTE 1 Refer to clause 6.28 for error function usage model. The host can erase the error log registers (Table 109, Register 0x04 to Table 112, Register 0x07) by writing 0x74 to Table 162, Register 0x39.
- NOTE 2 To exit from Error Injection Mode, the PMIC must go through power cycle of both VIN_Bulk and VIN_Mgmt input supply.
- NOTE 3 Error injection function utilizes two registers: Table 159, Register 0x35 and Table 193, Register 0x12F.
- NOTE 4 When error function is invoked by setting bit [7] = '1', the setting of bits Table 159, Register 0x35 [6:4, 2:0] = '000 000' and Table 193, Register 0x12F [5:4, 1:0] = '00 00' is considered an illegal setting.
- NOTE 5 The register Table 159, Register 0x35 [6:4] and Table 193, Register 0x12F [5:4] is only applicable if Table 159, Register 0x35 [2:0] is '000' and Table 193, Register 0x12F [1:0] = '00'. Any value other than '000' in Table 159, Register 0x35 [6:4], '00' in Table 193, Register 0x12F [5:4], '000' in Table 159, Register 0x35 [2:0] and '00' in Table 193, Register 0x12F [1:0] is considered an illegal setting and PMIC operation is not guaranteed.
- NOTE 6 If dual or three phase regulator is selected for SWA, SWB and SWE, use SWA encoding to inject the error. If dual phase regulator is selected for SWC and SWF, use SWC encoding to inject the error. Register Table 159, Register 0x35 [3] selects either over voltage or under voltage condition for the setting selected in this register.
- NOTE 7 This register Table 159, Register 0x35 [3] is only applicable if bits Table 159, Register 0x35 [6:4] and Table 193, Register 0x12F [5:4] is anything other than '000' and '00' respectively and Table 193, Register 0x12F [1:0] = '00'.
- NOTE 8 The under voltage selection only applies to SWx output rails and VIN_Bulk input. Does not apply to VIN_Mgmt input.
- NOTE 9 This register Table 159, Register 0x35 [2:0] is only applicable if Table 159, Register 0x35 [6:3] is '0000' and Table 193, Register 0x12F [5:4, 1:0] is '0000'. Any value other than '0000' in Table 159, Register 0x35 [6:3], '00' in Table 193, Register 0x12F [5:4], '000' in Table 159, Register 0x35 [2:0] and '00' in Table 193, Register 0x12F [1:0] is considered an illegal setting and PMIC operation is not guaranteed.
- NOTE 10 Applies to all enabled SWx output regulators at the same time.

11.4.5 Password Input and Command Code

Table 160 — Register 0x37

| R37 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description |
| 7:0 | WO | - | R37 [7:0]: DIMM_VENDOR_MEMORY_REGION_PASSWORD_LOWER_BYTE DIMM Vendor Memory Region (0x40 - 0x6F) Password - Lower Byte [7:0] = Code |

Table 161 — Register 0x38

| R38 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description |
| 7:0 | WO | - | R38 [7:0]: DIMM_VENDOR_MEMORY_REGION_PASSWORD_UPPER_BYTE DIMM Vendor Memory Region (0x40 - 0x6F) Password - Upper Byte [7:0] = Code |

Table 162 — Register 0x39

| R39 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description |
| 7:0 | RW | 0x00 | <p>R39 Codes:</p> <p>Host Region Codes:</p> <p>0x74: Clear Registers R04[7:4], R05 [7:0] to R07[7:0], Erase MTP memory for R04[7:4], R05[7:0] to R07[7:0]</p> <p>DIMM Vendor Region (0x40 to 0x6F) Write Codes:</p> <p>0x40: Unlock DIMM Vendor Region. Password needs to be present in R37 & R38 registers.</p> <p>0x00: Lock DIMM Vendor Region.</p> <p>0x80: Burn DIMM Vendor Region Password. New password needs to be present in R37 & R38.</p> <p>0x81: Burn DIMM Vendor Region - 0x40 to 0x4F</p> <p>0x82: Burn DIMM Vendor Region - 0x50 to 0x5F</p> <p>0x85: Burn DIMM Vendor Region - 0x60 to 0x6F</p> <p>DIMM Vendor Region (0x40 to 0x6F) Read Codes:</p> <p>0x5A: Burning is complete in DIMM Vendor region.</p> |

11.4.6 Miscellaneous Registers

Table 163 — Register 0x3A

| Bits | R3A | | |
|------|-----------|---------|---|
| | Attribute | Default | Description ^[1] |
| 7 | RV | 0 | R3A [7]: Reserved |
| 6 | RW | 0 | R3A [6]: DEFAULT_READ_ADDRESS_POINTER_ENABLE Enable Default Address Read Pointer when PMIC sees STOP operation 0 = Disable Default Address Pointer (address pointer is set by Host) ^[2] 1 = Enable Default Address Pointer; Address selected by register bits [5:4] ^[3] |
| 5:4 | RW | 0 | R3A [5:4]: DEFAULT_READ_STARTING_ADDRESS Default Read Address Pointer Selection when PMIC sees STOP operation ^[4] 00 = R08 01 = R0C 10 = R100 11 = Reserved |
| 3:2 | RW | 0 | R3A [3:2]: BURST_LENGTH_FOR_READ_DEFAULT_ADDR_POINTER Burst Length (# of Bytes) to be transferred for Read Default Address Pointer Mode ^[5] 00 = 2 Bytes 01 = 4 Bytes 10 = 8 Bytes 11 = 16 Bytes |
| 1 | RW | 0 | R3A [1]: BYPASS_DIMM_VENDOR_REGION_CRC_ERROR Bypass DIMM Vendor Region CRC Error for VR Enable 0 = Disable; PMIC blocks VR Enable command if Table 177, Register 0x10A [6] = '1' 1 = Enable; Ignore Table 177, Register 0x10A [6] Error status and turn on output regulators at next VR Enable command |
| 0 | 1O | 0 | R3A [0]: CHECK_DIMM_VENDOR_REGION_CRC Check DIMM Vendor Region CRC Code ^[6] 0 = No Action 1 = Check DIMM Vendor Region CRC Code |

- NOTE 1 The write (or update) transaction to this register must be followed by STOP operation to allow the PMIC device to update the setting.
- NOTE 2 The register setting in [Table 163, Register 0x3A](#)[5:4] is a don't care.
- NOTE 3 This mode is only allowed when PEC function is disabled (i.e., register [Table 158, Register 0x34](#)[7] = '0').
- NOTE 4 This register is only applicable if [Table 163, Register 0x3A](#)[6] = '1'.
- NOTE 5 This register is only applicable if [Table 163, Register 0x3A](#)[6] = '1' and [Table 158, Register 0x34](#)[7] = '1'.
- NOTE 6 The PMIC self clears this bit when CRC check is complete.

11.4.6 Miscellaneous Registers (cont'd)**Table 164 — Register 0x3B**

| R3B | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description |
| 7:6 | ROA | 10 | R3B [7:6]: PMIC_PART_CAPABILITY_EXT PMIC Current Capability Extension. This register bits [7:6] and bit [0] provides 3 bit encoding as following: 000 = PMIC5010 001 = PMIC5000 01x = PMIC5020 10x = PMIC5030 11x = Reserved |
| 5:4 | ROA | - | R3B [5:4]: REVISION_ID_MAJOR_STEPPING Major Revision Stepping 00 = Revision 1 01 = Revision 2 10 = Revision 3 11 = Revision 4 |
| 3:1 | ROA | - | R3B [3:1]: REVISION_ID_MINOR_STEPPING Minor Revision Stepping 000 = Revision 0 001 = Revision 1 010 = Revision 2 011 = Revision 3 All other encodings are reserved. |
| 0 | ROA | 0 | R3B [0]: PMIC_PART_CAPABILITY PMIC Current Capability. See also bits [7:6] definition. 0 = PMIC5010 1 = PMIC5000 |

Table 165 — Register 0x3C

| R3C | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description |
| 7:0 | ROA | - | R3C [7:0]: VENDOR_ID_BYTE0 Vendor Identification Register Byte 0. |

11.4.6 Miscellaneous Registers (cont'd)

Table 166 — Register 0x3D

| R3D | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description |
| 7:0 | ROA | - | R3D [7:0]: VENDOR_ID_BYTE1 Vendor Identification Register Byte 1. |

Table 167 — Register 0x100

| R100 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7:6 | RO | - | R100 [7:6]: SWA_OUTPUT_CURRENT_POWER_MEASUREMENT_MSB MSB bits - SWA Output Current or Output Power Measurement ^{[3],[4],[5]} These two MSB bits plus 8 bit register in Table 169, Register 0x102 [7:0] makes 10 bit encoding as shown in Table 169, Register 0x102 . |
| 5:4 | RO | - | R100 [5:4]: SWB_OUTPUT_CURRENT_POWER_MEASUREMENT_MSB MSB bits - SWB Output Current or Output Power Measurement ^{[2],[3],[4]} These two MSB bits plus 8 bit register in Table 170, Register 0x103 [7:0] makes 10 bit encoding as shown in Table 170, Register 0x103 . |
| 3:2 | RO | - | R100 [3:2]: SWC_OUTPUT_CURRENT_POWER_MEASUREMENT_MSB MSB bits - SWC Output Current or Output Power Measurement ^{[2],[3],[4]} These two MSB bits plus 8 bit register in Table 171, Register 0x104 [7:0] makes 10 bit encoding as shown in Table 171, Register 0x104 . |
| 1:0 | RO | - | R100 [1:0]: SWD_OUTPUT_CURRENT_POWER_MEASUREMENT_MSB MSB bits - SWD Output Current or Output Power Measurement ^{[2],[3],[4]} These two MSB bits plus 8 bit register in Table 172, Register 0x105 [7:0] makes 10 bit encoding as shown in Table 172, Register 0x105 . |

NOTE 1 This register is only applicable if [Table 155, Register 0x32](#) [1:0] = '01'.

NOTE 2 The Host must read ADC current or power measurement bytes in order from MSB to LSB (i.e., R100 to R107) via I²C/I³C block read commands.

NOTE 3 This register is only applicable if [Table 131, Register 0x1A](#) [1] = '0'

NOTE 4 The PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers VR Disable command, PMIC does not report current or power measurement and register content may have stale data. For all other events that causes PMIC's power good status as Not Good, the PMIC continues to provide current or power measurement.

NOTE 5 If [Table 132, Register 0x1B](#) [6] = '0', the PMIC reports current measurement. If [Table 132, Register 0x1B](#) [6] = '1', the PMIC reports power measurement.

11.4.6 Miscellaneous Registers (cont'd)

Table 168 — Register 0x101

| R101 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7:6 | RO | - | R101 [7:6]: SWE_OUTPUT_CURRENT_POWER_MEASUREMENT_MSB MSB bits - SWE Output Current or Output Power Measurement ^{[3],[4],[5]} These two MSB bits plus 8 bit register in Table 173, Register 0x106 [7:0] makes 10 bit encoding as shown in Table 173, Register 0x106 . |
| 5:4 | RO | - | R101 [5:4]: SWF_OUTPUT_CURRENT_POWER_MEASUREMENT_MSB MSB bits - SWF Output Current or Output Power Measurement ^{[2],[3],[4]} These two MSB bits plus 8 bit register in Table 174, Register 0x107 [7:0] makes 10 bit encoding as shown in Table 174, Register 0x107 . |
| 3 | RV | - | R101 [3]: Reserved |
| 2:0 | RO | - | R101 [2:0]: TOTAL_SWX_OUTPUT_POWER_MSB MSB bits - Total SWA+SWB+SWC+SWD+SWE+SWF Output Power Measurement ^{[6],[7]} These three MSB bits plus 8 bit register in Table 169, Register 0x102 [7:0] makes 11 bit encoding as shown in Table 169, Register 0x102 . |

NOTE 1 This register is only applicable if [Table 155, Register 0x32](#) [1:0] = '01'.

NOTE 2 The Host must read ADC current or power measurement bytes in order from MSB to LSB (i.e., R100 to R107) via I²C/I³C block read commands.

NOTE 3 This register is only applicable if [Table 131, Register 0x1A](#) [1] = '0'

NOTE 4 The PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers VR Disable command, PMIC does not report current or power measurement and register content may have stale data. For all other events that causes PMIC's power good status as Not Good, the PMIC continues to provide current or power measurement.

NOTE 5 If [Table 132, Register 0x1B](#) [6] = '0', the PMIC reports current measurement. If [Table 132, Register 0x1B](#) [6] = '1', the PMIC reports power measurement.

NOTE 6 This register is only applicable if [Table 131, Register 0x1A](#) [1] = '1'

NOTE 7 The PMIC reports power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers VR Disable command, PMIC does not report power measurement and register content may have stale data. For all other events that cause PMIC's power good status as Not Good, the PMIC continues to provide power measurement.

11.4.6 Miscellaneous Registers (cont'd)

Table 169 — Register 0x102

| R102 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7:0 | RO | - | <p>R102 [7:0]: SWA_OUTPUT_CURRENT_POWER_OR_TOTAL_POWER_MEASUREMENT_LSB</p> <p>If Table 131, Register 0x1A[1] = '0': ^{[3],[4]}</p> <p>LSB bits - SWA Output Current or Output Power. The 2 MSB bits Table 167, Register 0x100 [7:6] plus this 8 bit register makes 10 bit encoding as shown below.</p> <p>00 0000 0000 = Undefined</p> <p>00 0000 0001 = 31.25mA or 31.25mW</p> <p>00 0000 0010 = 62.5mA or 62.5mW</p> <p>...</p> <p>11 1111 1111 \geq 31.968A or 31.968W</p> <p>If Table 131, Register 0x1A[1] = '1': ^{[5],[6]}</p> <p>LSB bits - Total SWA+SWB+SWC+SWD+SWE+SWF Output Power. The 3 MSB bits Table 168, Register 0x101 [2:0] plus this 8 bit register makes 11 bit encoding as shown below.</p> <p>000 0000 0000 = Undefined</p> <p>000 0000 0001 = 31.25mW</p> <p>000 0000 0010 = 62.5mW</p> <p>...</p> <p>111 1111 1111 \geq 63.968W</p> |

NOTE 1 This register is only applicable if [Table 155, Register 0x32](#) [1:0] = '01'.

NOTE 2 The Host must read ADC current or power measurement bytes in order from MSB to LSB (i.e., R100 to R107) via I²C/I³C block read commands.

NOTE 3 The PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers VR Disable command, PMIC does not report current or power measurement and register content may have stale data. For all other events that causes PMIC's power good status as Not Good, the PMIC continues to provide current or power measurement.

NOTE 4 If [Table 132, Register 0x1B](#) [6] = '0', the PMIC reports current measurement. If [Table 132, Register 0x1B](#) [6] = '1', the PMIC reports power measurement.

NOTE 5 The PMIC reports power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers VR Disable command, PMIC does not report power measurement and register content may have stale data. For all other events that cause PMIC's power good status as Not Good, the PMIC continues to provide power measurement.

NOTE 6 The register [Table 132, Register 0x1B](#) [6] must be configured as '1'.

11.4.6 Miscellaneous Registers (cont'd)

Table 170 — Register 0x103

| R103 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7:0 | RO | - | <p>R103 [7:0]: SWB_OUTPUT_CURRENT_POWER_MEASUREMENT_LSB LSB bits - SWB Output Current or Output Power Measurement^{[3],[4]}</p> <p>The 2 MSB bits Table 167, Register 0x100 [5:4] plus this 8 bit register makes 10 bit encoding as shown below.</p> <p>Table 131, Register 0x1A[1] = '0': 00 0000 0000 = Undefined 00 0000 0001 = 31.25mA or 31.25mW 00 0000 0010 = 62.5mA or 62.5mW ... 11 1111 1111 \geq 31.968A or 31.968W</p> |

NOTE 1 This register is only applicable if [Table 155, Register 0x32](#) [1:0] = '01'.

NOTE 2 The Host must read ADC current or power measurement bytes in order from MSB to LSB (i.e., R100 to R107) via I²C/I³C block read commands.

NOTE 3 The PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers VR Disable command, PMIC does not report current or power measurement and register content may have stale data. For all other events that causes PMIC's power good status as Not Good, the PMIC continues to provide current or power measurement.

NOTE 4 If [Table 132, Register 0x1B](#) [6] = '0', the PMIC reports current measurement. If [Table 132, Register 0x1B](#) [6] = '1', the PMIC reports power measurement.

Table 171 — Register 0x104

| R104 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7:0 | RO | - | <p>R104 [7:0]: SWC_OUTPUT_CURRENT_POWER_MEASUREMENT_LSB LSB bits - SWC Output Current or Output Power Measurement^{[3],[4]}</p> <p>The 2 MSB bits Table 167, Register 0x100 [3:2] plus this 8 bit register makes 10 bit encoding as shown below.</p> <p>Table 131, Register 0x1A[1] = '0': 00 0000 0000 = Undefined 00 0000 0001 = 31.25mA or 31.25mW 00 0000 0010 = 62.5mA or 62.5mW ... 11 1111 1111 \geq 31.968A or 31.968W</p> |

NOTE 1 This register is only applicable if [Table 155, Register 0x32](#) [1:0] = '01'.

NOTE 2 The Host must read ADC current or power measurement bytes in order from MSB to LSB (i.e., R100 to R107) via I²C/I³C block read commands.

NOTE 3 The PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers VR Disable command, PMIC does not report current or power measurement and register content may have stale data. For all other events that causes PMIC's power good status as Not Good, the PMIC continues to provide current or power measurement.

NOTE 4 If [Table 132, Register 0x1B](#) [6] = '0', the PMIC reports current measurement. If [Table 132, Register 0x1B](#) [6] = '1', the PMIC reports power measurement.

11.4.6 Miscellaneous Registers (cont'd)

Table 172 — Register 0x105

| R105 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7:0 | RO | - | <p>R105 [7:0]: SWD_OUTPUT_CURRENT_POWER_MEASUREMENT_LSB LSB bits - SWD Output Current or Output Power Measurement^{[3],[4]}</p> <p>The 2 MSB bits Table 167, Register 0x100 [1:0] plus this 8 bit register makes 10 bit encoding as shown below.</p> <p>Table 131, Register 0x1A[1] = '0': 00 0000 0000 = Undefined 00 0000 0001 = 31.25mA or 31.25mW 00 0000 0010 = 62.5mA or 62.5mW ... 11 1111 1111 ≥ 31.968A or 31.968W</p> |

NOTE 1 This register is only applicable if [Table 155, Register 0x32](#) [1:0] = '01'.

NOTE 2 The Host must read ADC current or power measurement bytes in order from MSB to LSB (i.e., R100 to R107) via I²C/I³C block read commands.

NOTE 3 The PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers VR Disable command, PMIC does not report current or power measurement and register content may have stale data. For all other events that causes PMIC's power good status as Not Good, the PMIC continues to provide current or power measurement.

NOTE 4 If [Table 132, Register 0x1B](#) [6] = '0', the PMIC reports current measurement. If [Table 132, Register 0x1B](#) [6] = '1', the PMIC reports power measurement.

Table 173 — Register 0x106

| R106 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7:0 | RO | - | <p>R106 [7:0]: SWE_OUTPUT_CURRENT_POWER_MEASUREMENT_LSB LSB bits - SWE Output Current or Output Power Measurement^{[3],[4]}</p> <p>The 2 MSB bits Table 168, Register 0x101 [7:6] plus this 8 bit register makes 10 bit encoding as shown below.</p> <p>Table 131, Register 0x1A[1] = '0': 00 0000 0000 = Undefined 00 0000 0001 = 31.25mA or 31.25mW 00 0000 0010 = 62.5mA or 62.5mW ... 11 1111 1111 ≥ 31.968A or 31.968W</p> |

NOTE 1 This register is only applicable if [Table 155, Register 0x32](#) [1:0] = '01'.

NOTE 2 The Host must read ADC current or power measurement bytes in order from MSB to LSB (i.e., R100 to R107) via I²C/I³C block read commands.

NOTE 3 The PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers VR Disable command, PMIC does not report current or power measurement and register content may have stale data. For all other events that causes PMIC's power good status as Not Good, the PMIC continues to provide current or power measurement.

NOTE 4 If [Table 132, Register 0x1B](#) [6] = '0', the PMIC reports current measurement. If [Table 132, Register 0x1B](#) [6] = '1', the PMIC reports power measurement.

11.4.6 Miscellaneous Registers (cont'd)

Table 174 — Register 0x107

| R107 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7:0 | RO | - | <p>R107 [7:0]: SWF_OUTPUT_CURRENT_POWER_MEASUREMENT_LSB LSB bits - SWF Output Current or Output Power Measurement^{[3],[4]}</p> <p>The 2 MSB bits Table 168, Register 0x101 [5:4] plus this 8 bit register makes 10 bit encoding as shown below.</p> <p>Table 131, Register 0x1A [1] = '0': 00 0000 0000 = Undefined 00 0000 0001 = 31.25mA or 31.25mW 00 0000 0010 = 62.5mA or 62.5mW ... 11 1111 1111 ≥ 31.968A or 31.968W</p> |

NOTE 1 This register is only applicable if [Table 155, Register 0x32](#) [1:0] = '01'.

NOTE 2 The Host must read ADC current or power measurement bytes in order from MSB to LSB (i.e., R100 to R107) via I²C/I³C block read commands.

NOTE 3 The PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers VR Disable command, PMIC does not report current or power measurement and register content may have stale data. For all other events that causes PMIC's power good status as Not Good, the PMIC continues to provide current or power measurement.

NOTE 4 If [Table 132, Register 0x1B](#) [6] = '0', the PMIC reports current measurement. If [Table 132, Register 0x1B](#) [6] = '1', the PMIC reports power measurement.

Table 175 — Register 0x108

| R108 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description |
| 7 | RO | 0 | <p>R108 [7]: SWE_OUTPUT_POWER_GOOD_STATUS Switch Node E Output Power Good Status^{[1],[2]} 0 = Power Good 1 = Power Not Good</p> |
| 6 | RO | 0 | <p>R108 [6]: SWF_OUTPUT_POWER_GOOD_STATUS Switch Node F Output Power Good Status^{[3],[4]} 0 = Power Good 1 = Power Not Good</p> |
| 5 | RO | 0 | <p>R108 [5]: SWE_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Switch Node E High Output Current Consumption Warning Status^{[5],[6]} 0 = No High Current Consumption Warning 1 = High Current Consumption Warning</p> |

Table 175 — Register 0x108 (cont'd)

| R108 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description |
| 4 | RO | 0 | R108 [4]: SWF_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Switch Node F High Output Current Consumption Warning Status ^{[7],[8]} 0 = No High Current Consumption Warning 1 = High Current Consumption Warning |
| 3 | RO | 0 | R108 [3]: SWE_OUTPUT_OVER_VOLTAGE_STATUS Switch Node E Output Over Voltage Status ^{[1],[9]} 0 = No Over Voltage 1 = Over Voltage |
| 2 | RO | 0 | R108 [2]: SWF_OUTPUT_OVER_VOLTAGE_STATUS Switch Node F Output Over Voltage Status ^{[3],[10]} 0 = No Over Voltage 1 = Over Voltage |
| 1 | RO | 0 | R108 [1]: SWE_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node E Output Current Limiter Warning Status ^{[5],[11]} 0 = No Current Limiter Event 1 = Current Limiter Event |
| 0 | RO | 0 | R108 [0]: SWF_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node F Output Current Limiter Warning Status ^{[7],[12]} 0 = No Current Limiter Event 1 = Current Limiter Event |

- NOTE 1 Only applicable if [Table 247, Register 0x4F](#) [5,0] = '00' or '01'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.
- NOTE 2 This register is set when SWE output voltage goes either below the threshold setting in register [Table 185, Register 0x11D](#) [1:0] or above the threshold setting in register [Table 186, Register 0x11E](#) [7:6].
- NOTE 3 Only applicable if [Table 247, Register 0x4F](#) [6] = '0'. For any other setting in [Table 247, Register 0x4F](#) [6], this register does not apply and it is a don't care.
- NOTE 4 This register is set when SWF output goes either below the threshold setting in register [Table 187, Register 0x11F](#) [1:0] or above the threshold setting in register [Table 188, Register 0x120](#) [7:6].
- NOTE 5 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [5,0].
- NOTE 6 This register is set when SWE output current consumption goes above the threshold setting in [Table 182, Register 0x11A](#) [7:0].
- NOTE 7 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [6].
- NOTE 8 This register is set when SWF output current consumption goes above the threshold setting in [Table 183, Register 0x11B](#) [7:0].
- NOTE 9 This register is set when SWE output voltage goes above the threshold setting in [Table 186, Register 0x11E](#) [5:4].
- NOTE 10 This register is set when SWE output voltage goes above the threshold setting in [Table 188, Register 0x120](#) [5:4].
- NOTE 11 This register is set when SWE output current goes above the threshold setting in [Table 184, Register 0x11C](#) [7:6]. If [Table 247, Register 0x4F](#) [5,0] = '1x', the setting in [Table 137, Register 0x20](#) [5:4], [Table 137, Register 0x20](#) [7:6] and [Table 184, Register 0x11C](#) [7:6] must be configured identical.
- NOTE 12 This register is set when SWF output current goes above the threshold setting in [Table 184, Register 0x11C](#) [5:4]. If [Table 247, Register 0x4F](#) [6] = '1', the setting in [Table 137, Register 0x20](#) [3:2] must be identical as [Table 184, Register 0x11C](#) [5:4].

11.4.6 Miscellaneous Registers (cont'd)

Table 176 — Register 0x109

| R109 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description |
| 7 | RO | 0 | R109 [7]: SWE_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node E Output Under Voltage Lockout Status ^{[1].[2]} 0 = No Under Voltage Lockout 1 = Under Voltage Lockout |
| 6 | RO | 0 | R109 [6]: SWF_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node F Output Under Voltage Lockout Status ^{[3].[4]} 0 = No Under Voltage Lockout 1 = Under Voltage Lockout |
| 5:1 | RV | 0 | R109 [5:1]: Reserved |
| 0 | RO | 0 | R109 [0]: DIMM_VENDOR_REGION_CRC_CHECK_ON_CMD_STATUS DIMM Vendor Region CRC Check on CMD; i.e., Table 163, Register 0x3A [0] = '1' 0 = DIMM Region CRC Error Checked - No Error 1 = DIMM Region CRC Error Checked - Error |

NOTE 1 Only applicable if [Table 247, Register 0x4F](#) [5,0] = '00' or '01'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 2 This register is set when SWE output voltage goes below the threshold setting in [Table 186, Register 0x11E](#) [3:2].

NOTE 3 Only applicable if [Table 247, Register 0x4F](#) [6] = '1'. For any other setting in [Table 247, Register 0x4F](#) [6], this register does not apply and it is a don't care.

NOTE 4 This register is set when SWF output voltage goes below the threshold setting in [Table 188, Register 0x120](#) [3:2].

11.4.6 Miscellaneous Registers (cont'd)

Table 177 — Register 0x10A

| Bits | R10A | | |
|------|-----------|---------|--|
| | Attribute | Default | Description |
| 7 | RO | 0 | R10A [7]: DIMM_VENDOR_REGION_MTP_CRC_CHECK_STATUS DIMM Vendor Region MTP CRC Check Status at first power on ^[1] 0 = DIMM Region MTP CRC Not Checked 1 = DIMM Region MTP CRC Checked |
| 6 | RO | 0 | R10A [6]: DIMM_VENDOR_REGION_MTP_CRC_CHECK_ERROR_STATUS DIMM Vendor Region MTP CRC Check Error Status at first power on ^[2] 0 = DIMM Region MTP CRC Error Checked - No Error 1 = DIMM Region MTP CRC Error Checked - Error |
| 5 | RO | 0 | R10A [5]: PMIC_VENDOR_REGION_MTP_CHECK_STATUS PMIC Vendor Region MTP Check Status at first power on ^[3] 0 = PMIC Region MTP Error Not Checked 1 = PMIC Region MTP Error Checked |
| 4 | RO | 0 | R10A [4]: PMIC_VENDOR_REGION_MTP_CHECK_ERROR_STATUS PMIC Vendor Region MTP Check Error Status at first power on ^[4] 0 = PMIC Region MTP Error Checked - No Error 1 = PMIC Region MTP Error Checked - Error |
| 3:0 | RV | 0 | R10A [3:0]: Reserved |

- NOTE 1 PMIC must check the DIMM Vendor Region MTP for error as defined in clause 6.30 and sets this bit [7] to '1' after checking. If PMIC does not perform the DIMM vendor region MTP error check at power on, the PMIC keeps this bit to '0'.
- NOTE 2 This bit is only applicable if bit [7] is set to '1'. After PMIC checks for DIMM region MTP error, the PMIC sets this bit [6] to '1' if there is an error.
- NOTE 3 PMIC must check the PMIC Vendor Region MTP for error as defined in clause 6.30 and set this bit [5] to '1' after checking. If PMIC does not perform the PMIV vendor region MTP error check at power on, the PMIC keeps this bit to '0'.
- NOTE 4 This bit is only applicable if bit [5] is set to '1'. After PMIC checks for PMIC vendor region MTP error, the PMIC sets this bit [4] to '1' if there is an error.

11.4.6 Miscellaneous Registers (cont'd)

Table 178 — Register 0x10E

| R10E | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^[1] |
| 7 | 10 | 0 | R10E [7]: CLEAR_SWE_OUTPUT_POWER_GOOD_STATUS Clear SWE Output Power Good Status. ^[2] 1 = Clear Register Table 175, Register 0x108 [7] ^[3] |
| 6 | 10 | 0 | R10E [6]: CLEAR_SWF_OUTPUT_POWER_GOOD_STATUS Clear SWF Output Power Good Status. ^[4] 1 = Clear Register Table 175, Register 0x108 [6] ^[3] |
| 5 | 10 | 0 | R10E [5]: CLEAR_SWE_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Clear Switch Node E High Output Current Consumption Warning Status. ^[5] 1 = Clear Register Table 175, Register 0x108 [5] ^[3] |
| 4 | 10 | 0 | R10E [4]: CLEAR_SWF_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Clear Switch Node F High Output Current Consumption Warning Status. ^[6] 1 = Clear Register Table 175, Register 0x108 [4] ^[3] |
| 3 | 10 | 0 | R10E [3]: CLEAR_SWE_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node E Output Over Voltage Status. ^[2] 1 = Clear Register Table 175, Register 0x108 [3] ^[3] |
| 2 | 10 | 0 | R10E [2]: CLEAR_SWF_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node F Output Over Voltage Status. ^[4] 1 = Clear Register Table 175, Register 0x108 [2] ^[3] |
| 1 | 10 | 0 | R10E [1]: CLEAR_SWE_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Clear Switch Node E Output Current Limiter Warning Status. ^[5] 1 = Clear Register Table 175, Register 0x108 [1] ^[3] |
| 0 | 10 | 0 | R10E [0]: CLEAR_SWF_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Clear Switch Node F Output Current Limiter Warning Status. ^[6] 1 = Clear Register Table 175, Register 0x108 [0] ^[3] |

NOTE 1 [Table 178, Register 0x10E](#) [7:0] are self-clearing bits.

NOTE 2 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00' or '01'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 3 See [Table 28](#) and [Table 29](#) for GSI_n and POWER_GOOD output signal status change.

NOTE 4 This register is only applicable if [Table 247, Register 0x4F](#) [6] = '0'. For any other setting in [Table 247, Register 0x4F](#) [6], this register does not apply and it is a don't care.

NOTE 5 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [5,0].

NOTE 6 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [6].

11.4.6 Miscellaneous Registers (cont'd)

Table 179 — Register 0x10F

| R10F | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description ^[1] |
| 7 | 1O | 0 | R10F [7]: CLEAR_SWE_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Clear Switch Node E Output Under Voltage Lockout Status. ^[2] 1 = Clear Register Table 176, Register 0x109 [7] ^[3] |
| 6 | 1O | 0 | R10F [6]: CLEAR_SWF_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Clear Switch Node F Output Under Voltage Lockout Status. ^[4] 1 = Clear Register Table 176, Register 0x109 [6] ^[3] |
| 5:1 | RV | 0 | R10F [5:1]: Reserved |
| 0 | 1O | 0 | R10F [0]: CLEAR_DIMM_REGION_CRC_ERROR_STATUS Clear DIMM Vendor Region CRC Error Status 1 = Clear Register Table 176, Register 0x109 [0] |

NOTE 1 [Table 179, Register 0x10F](#) [7:0] are self-clearing bits.

NOTE 2 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00' or '01'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 3 See [Table 28](#) and [Table 29](#) for GSI_n and POWER_GOOD output signal status change.

NOTE 4 This register is only applicable if [Table 247, Register 0x4F](#) [6] = '0'. For any other setting in [Table 247, Register 0x4F](#) [6], this register does not apply and it is a don't care.

11.4.6 Miscellaneous Registers (cont'd)

Table 180 — Register 0x114

| R114 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description |
| 7 | RW | 1 | R114 [7]: MASK_SWE_OUTPUT_POWER_GOOD_STATUS Mask SWE Output Power Good Status Event. ^[1] 0 = Do Not Mask SWE Output Power Good Status Event 1 = Mask SWE Output Power Good Status Event ^[2] |
| 6 | RW | 1 | R114 [6]: MASK_SWF_OUTPUT_POWER_GOOD_STATUS Mask SWF Output Power Good Status Event. ^[3] 0 = Do Not Mask SWF Output Power Good Status Event 1 = Mask SWF Output Power Good Status Event ^[2] |
| 5 | RW | 0 | R114 [5]: MASK_SWE_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Mask SWE High Output Current Consumption Warning Status Event. ^[1] 0 = Do Not Mask SWE Output Current Consumption Warning Status Event 1 = Mask SWE Output Current Consumption Warning Status Event ^[4] |
| 4 | RW | 0 | R114 [4]: MASK_SWF_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Mask SWF High Output Current Consumption Warning Status Event. ^[3] 0 = Do Not Mask SWF Output Current Consumption Warning Status Event 1 = Mask SWF Output Current Consumption Warning Status Event ^[4] |
| 3 | RW | 0 | R114 [3]: MASK_SWE_OUTPUT_OVER_VOLTAGE_STATUS Mask SWE Output Over Voltage Status Event. ^[1] 0 = Do Not Mask SWE Output Over Voltage Status Event 1 = Mask SWE Output Over Voltage Status Event ^[4] |
| 2 | RW | 0 | R114 [2]: MASK_SWF_OUTPUT_OVER_VOLTAGE_STATUS Mask SWF Output Over Voltage Status Event. ^[3] 0 = Do Not Mask SWF Output Over Voltage Status Event 1 = Mask SWF Output Over Voltage Status Event ^[4] |
| 1 | RW | 0 | R114 [1]: MASK_SWE_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Mask SWE Output Current Limiter Warning Status Event. ^[1] 0 = Do Not Mask SWE Output Current Limiter Warning Status Event 1 = Mask SWE Output Current Limiter Warning Status Event ^[4] |
| 0 | RW | 0 | R114 [0]: MASK_SWF_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Mask SWF Output Current Limiter Warning Status Event. ^[3] 0 = Do Not Mask SWF Output Current Limiter Warning Status Event 1 = Mask SWF Output Current Limiter Warning Status Event ^[4] |

NOTE 1 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00' or '01'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 2 Not assert GSI_n or PWR_GOOD output signal.

NOTE 3 This register is only applicable if [Table 247, Register 0x4F](#) [6] = '0'. For any other setting in [Table 247, Register 0x4F](#) [6], this register does not apply and it is a don't care.

NOTE 4 Not assert GSI_n output signal.

11.4.6 Miscellaneous Registers (cont'd)

Table 181 — Register 0x115

| R115 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description |
| 7 | RW | 0 | R115 [7]: MASK_SWE_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Mask SWE Output Under Voltage Lockout Status Event. ^[1] 0 = Do Not Mask SWE Output Under Voltage Lockout Status Event 1 = Mask SWE Output Under Voltage Lockout Status Event ^[2] |
| 6 | RW | 0 | R115 [6]: MASK_SWF_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Mask SWF Output Under Voltage Lockout Status Event. ^[3] 0 = Do Not Mask SWF Output Under Voltage Lockout Status Event 1 = Mask SWF Output Under Voltage Lockout Status Event ^[2] |
| 5:0 | RV | 0 | R115 [5:0]: Reserved |

NOTE 1 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00' or '01'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 2 Not assert GSI_n output signal.

NOTE 3 This register is only applicable if [Table 247, Register 0x4F](#) [6] = '0'. For any other setting in [Table 247, Register 0x4F](#) [6], this register does not apply and it is a don't care.

Table 182 — Register 0x11A

| R11A | | | |
|------|-----------|--------------|--|
| Bits | Attribute | Default | Description ^[1] |
| 7:0 | RW | 0011 1100 | R11A [7:0]: SWE_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD SWE Output High Current Consumption Warning Threshold ^[2] If Table 155, Register 0x32 [1:0] = '00': 0000 0000 = Undefined 0000 0001 = > 125 mA 0000 0010 = > 250 mA ... 1111 1111 = > 31.875 A If Table 155, Register 0x32 [1:0] = '01': 0000 0000 = Undefined 0000 0001 = > 31.25 mA 0000 0010 = > 62.5 mA ... 1111 1111 = > 7.968 A |

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 275, Register 0x6B](#).

NOTE 2 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [5,0]. For three phase operation, registers [Table 133, Register 0x1C](#) [7:0], [Table 134, Register 0x1D](#) [7:0] and [Table 182, Register 0x11A](#) [7:0] must be configured identical.

11.4.6 Miscellaneous Registers (cont'd)

Table 183 — Register 0x11B

| R11B | | | |
|------|-----------|--------------|---|
| Bits | Attribute | Default | Description ^[1] |
| 7:0 | RW | 0011 1100 | <p>R11B [7:0]: SWF_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD SWF Output High Current Consumption Warning Threshold^[2]</p> <p>If Table 155, Register 0x32[1:0] = '00': 0000 0000 = Undefined 0000 0001 = > 125 mA 0000 00100 = > 250 mA ... 1111 1111 = > 31.875 A</p> <p>If Table 155, Register 0x32[1:0] = '01': 0000 0000 = Undefined 0000 0001 = > 31.25 mA 0000 0010 = > 62.5 mA ... 1111 1111 = > 7.968 A</p> |

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 276, Register 0x6C](#).

NOTE 2 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [6]. For dual phase operation, registers [Table 135, Register 0x1E](#) [7:0] and [Table 183, Register 0x11B](#) [7:0] must be configured identical.

11.4.6 Miscellaneous Registers (cont'd)

Table 184 — Register 0x11C

| Bits | R11C | | |
|------|-----------|---------|--|
| | Attribute | Default | Description ^[1] |
| 7:6 | RW | 01 | R11C [7:6]: SWE_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING COT lvalley_limit ^[2] 00 = 6A 01 = 7A 10 = 8A 11 = 9A |
| 5:4 | RW | 01 | R11C [5:4]: SWF_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING COT lvalley_limit ^[3] 00 = 6A 01 = 7A 10 = 8A 11 = 9A |
| 3 | RW | 0 | R11C [3]: SWE_VOLTAGE_RANGE SWE Output Voltage Range Selection ^{[4],[5]} 0 = Range: 800 mV to 1435 mV for SWA; 5 mV step size 1 = Range: 600 mV to 1235 mV for SWA; 5 mV step size |
| 2:1 | RW | 0 | R11C [2:1]: SWF_VOLTAGE_RANGE SWF Output Voltage Range Selection ^{[6],[7]} 00 = Range: 800 mV to 1435 mV for SWF; 5 mV step size 01 = Range: 600 mV to 1235 mV for SWF; 5 mV step size 10 = Range: 400 mV to 717.5 mV for SWF; 2.5 mV step size 11 = Reserved |
| 0 | RW | 0 | R11C [0]: SWC_VOLTAGE_RANGE_EXT SWC Output Voltage Range Selection ^[8] . The MSB bit Table 184, Register 0x11C [0] plus LSB bit Table 148, Register 0x2B [3] makes 2 bit encoding as following: 00 = Range: 800 mV to 1435 mV for SWC; 5 mV step size 01 = Range: 600 mV to 1235 mV for SWC; 5 mV step size 10 = Range: 400 mV to 717.5 mV for SWC; 2.5 mV step size 11 = Reserved |

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 250, Register 0x52](#).

NOTE 2 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [5,0].

NOTE 3 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [6].

NOTE 4 Range and resolution selection applies to register [Table 185, Register 0x11D](#) [7:1].

NOTE 5 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00' or '01'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 6 Range and resolution selection applies to register [Table 187, Register 0x11F](#) [7:1].

NOTE 7 This register is only applicable if [Table 247, Register 0x4F](#) [6] = '0'. For any other setting in [Table 247, Register 0x4F](#) [6], this register does not apply and it is a don't care.

NOTE 8 Range selection applies to registers [Table 142, Register 0x25](#) [7:1].

11.4.6 Miscellaneous Registers (cont'd)

Table 185 — Register 0x11D

| R11D | | | |
|------|-----------|----------|--|
| Bits | Attribute | Default | Description ^{[1],[2],[3]} |
| 7:1 | RW | 011 1100 | R11D [7:1]: SWE_VOLTAGE_SETTING SWE Output Regulator Voltage Setting ^{[4],[5]} 000 0000 = 800 mV ^[6] or 600 mV ^[7] 000 0001 = 805 mV or 605 mV 000 0010 = 810 mV or 610 mV ... 011 1100 = 1100 mV or 900 mV ... 111 1101 = 1425 mV or 1225 mV 111 1110 = 1430 mV or 1230 mV 111 1111 = 1435 mV or 1235 mV |
| 0 | RW | 0 | R11D [0]: SWE_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING SWE Output Threshold Low Side Voltage For Power Good Status 0 = -5% from the setting in Table 185, Register 0x11D [7:1] 1 = -7.5% from the setting in Table 185, Register 0x11D [7:1] |

- NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 251, Register 0x53](#).
- NOTE 2 If required, the host must update the settings in register [Table 185, Register 0x11D \[0\]](#), [Table 185, Register 0x11D \[7:2\]](#) and [Table 184, Register 0x11C \[7:6\]](#) first prior to updating the settings in the register [Table 185, Register 0x11D \[7:1\]](#).
- NOTE 3 This register is only applicable if [Table 247, Register 0x4F \[5,0\]](#) = '00' or '01'. For any other setting in [Table 247, Register 0x4F \[5,0\]](#), this register does not apply and it is a don't care.
- NOTE 4 PMIC guarantees efficiency spec within a range of 1050 mV to 1160 mV.
- NOTE 5 After VR is enabled, the host may update this register to any new setting that it may desire. However to prevent false error trigger, the PMIC internally will increment the SWE output voltage setting by 5 mV at a time. The time it takes for PMIC to adjust the output voltage is 5 μ s for each 5 mV increment. The host must wait sufficient time for PMIC to adjust to final value. As an example, if host adjusts the output voltage by 50 mV from the original value, the host must wait minimum of 50 μ s before PMIC can guarantee the new output voltage. During this time, PMIC masks the PWR_GOOD output signal assertion to prevent any artificial error due to the crossing of the output voltage threshold setting. However, PMIC does assert PWR_GOOD output signal if there are any abnormal issues that triggers VR Disable command as described in [Table 27](#). Further, PMIC does monitor PWR_GOOD input signal and executes power off config sequence registers if it is registered low when [Table 155, Register 0x32 \[5\]](#) = '1'.
- NOTE 6 [Table 184, Register 0x11C \[3\]](#) = '0'; 5 mV step size.
- NOTE 7 [Table 184, Register 0x11C \[3\]](#) = '1'; 5 mV step size

11.4.6 Miscellaneous Registers (cont'd)

Table 186 — Register 0x11E

| R11E | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description ^{[1],[2],[3]} |
| 7:6 | RW | 01 | R11E [7:6]: SWE_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING SWE Output Threshold High Side Voltage For Power Good Status 00 = +5% from the setting in Table 185, Register 0x11D [7:1] 01 = +7.5% from the setting in Table 185, Register 0x11D [7:1] 10 = +10% from the setting in Table 185, Register 0x11D [7:1] 11 = Reserved |
| 5:4 | RW | 10 | R11E [5:4]: SWE_OVER_VOLTAGE_THRESHOLD_SETTING SWE Output Regulator Threshold For Over Voltage Status ^[4] 00 = +7.5% from the setting in Table 185, Register 0x11D [7:1] 01 = +10% from the setting in Table 185, Register 0x11D [7:1] 10 = +12.5% from the setting in Table 185, Register 0x11D [7:1] 11 = Reserved |
| 3:2 | RW | 00 | R11E [3:2]: SWE_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING SWE Output Regulator Threshold For Under Voltage Lockout Status 00 = -10% from the setting in Table 185, Register 0x11D [7:1] 01 = -12.5% from the setting in Table 185, Register 0x11D [7:1] 10 = Reserved 11 = Reserved |
| 1:0 | RW | 00 | R11E [1:0]: SWE_OUTPUT_SOFT_STOP_TIME SWE Output Regulator Soft Stop Time After VR Disable ^[5] 00 = 0.5 ms 01 = 1 ms 10 = 2 ms 11 = 4 ms |

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 252, Register 0x54](#).

NOTE 2 If required, the host must update the setting in register [Table 185, Register 0x11D \[0\]](#), [Table 186, Register 0x11E \[7:2\]](#) and [Table 184, Register 0x11C \[7:6\]](#) first prior to updating the settings in the register [Table 185, Register 0x11D \[7:1\]](#).

NOTE 3 This register is only applicable if [Table 247, Register 0x4F \[5,0\]](#) = '00' or '01'. For any other setting in [Table 247, Register 0x4F \[5,0\]](#), this register does not apply and it is a don't care.

NOTE 4 The setting for the Over Voltage must be higher than Power Good High Side Voltage threshold in [Table 185, Register 0x11D \[7:6\]](#).

NOTE 5 This is the time it takes for buck regulator to go from steady state voltage to 0 V.

11.4.6 Miscellaneous Registers (cont'd)

Table 187 — Register 0x11F

| R11F | | | |
|------|-----------|----------|---|
| Bits | Attribute | Default | Description ^{[1],[2],[3]} |
| 7:1 | RW | 011 1100 | R11F [7:1]: SWF_VOLTAGE_SETTING SWF Output Regulator Voltage Setting ^{[4],[5]} 000 0000 = 800 mV ^[6] or 600 mV ^[7] or 400 mV ^[8] 000 0001 = 805 mV or 605 mV or 402.5 mV 000 0010 = 810 mV or 610 mV or 405 mV ... 011 1100 = 1100 mV or 900 mV or 550 mV ... 111 1101 = 1425 mV or 1225 mV or 712.5 mV 111 1110 = 1430 mV or 1230 mV or 715 mV 111 1111 = 1435 mV or 1235 mV or 717.5 mV |
| 0 | RW | 0 | R11F [0]: SWF_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING SWF Output Threshold Low Side Voltage For Power Good Status 0 = -5% from the setting in Table 187, Register 0x11F [7:1] 1 = -7.5% from the setting in Table 187, Register 0x11F [7:1] |

- NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 253, Register 0x55](#).
- NOTE 2 If required, the host must update the settings in register [Table 187, Register 0x11F \[0\]](#), [Table 188, Register 0x120 \[7:2\]](#) and [Table 184, Register 0x11C \[5:4\]](#) first prior to updating the settings in the register [Table 187, Register 0x11F \[7:1\]](#).
- NOTE 3 This register is only applicable if [Table 247, Register 0x4F \[6\]](#) = '0'. For any other setting in [Table 247, Register 0x4F \[6\]](#), this register does not apply and it is a don't care.
- NOTE 4 PMIC guarantees efficiency spec within a range of 1050 mV to 1160 mV.
- NOTE 5 After VR is enabled, the host may update this register to any new setting that it may desire. However to prevent false error trigger, the PMIC internally will increment the SWF output voltage setting by 5 mV at a time. The time it takes for PMIC to adjust the output voltage is 5 μ s for each 5 mV increment. The host must wait sufficient time for PMIC to adjust to final value. As an example, if host adjusts the output voltage by 50 mV from the original value, the host must wait minimum of 50 μ s before PMIC can guarantee the new output voltage. During this time, PMIC masks the PWR_GOOD output signal assertion to prevent any artificial error due to the crossing of the output voltage threshold setting. However, PMIC does assert PWR_GOOD output signal if there are any abnormal issues that triggers VR Disable command as described in [Table 27](#). Further, PMIC does monitor PWR_GOOD input signal and executes power off config sequence registers if it is registered low when [Table 155, Register 0x32 \[5\]](#) = '1'.
- NOTE 6 [Table 184, Register 0x11C \[2:1\]](#) = '00'; 5 mV step size.
- NOTE 7 [Table 184, Register 0x11C \[2:1\]](#) = '01'; 5 mV step size
- NOTE 8 [Table 184, Register 0x11C \[2:1\]](#) = '10'; 2.5 mV step size.

11.4.6 Miscellaneous Registers (cont'd)

Table 188 — Register 0x120

| R120 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description ^{[1],[2],[3]} |
| 7:6 | RW | 01 | R120 [7:6]: SWF_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING SWF Output Threshold High Side Voltage For Power Good Status 00 = +5% from the setting in Table 187, Register 0x11F [7:1] 01 = +7.5% from the setting in Table 187, Register 0x11F [7:1] 10 = +10% from the setting in Table 187, Register 0x11F [7:1] 11 = Reserved |
| 5:4 | RW | 10 | R120 [5:4]: SWF_OVER_VOLTAGE_THRESHOLD_SETTING SWF Output Regulator Threshold For Over Voltage Status ^[4] 00 = +7.5% from the setting in Table 187, Register 0x11F [7:1] 01 = +10% from the setting in Table 187, Register 0x11F [7:1] 10 = +12.5% from the setting in Table 187, Register 0x11F [7:1] 11 = Reserved |
| 3:2 | RW | 00 | R120 [3:2]: SWF_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING SWF Output Regulator Threshold For Under Voltage Lockout Status 00 = -10% from the setting in Table 187, Register 0x11F [7:1] 01 = -12.5% from the setting in Table 187, Register 0x11F [7:1] 10 = Reserved 11 = Reserved |
| 1:0 | RW | 00 | R120 [1:0]: SWF_OUTPUT_SOFT_STOP_TIME SWF Output Regulator Soft Stop Time After VR Disable ^[5] 00 = 0.5 ms 01 = 1 ms 10 = 2 ms 11 = 4 ms |

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 254, Register 0x56](#).

NOTE 2 If required, the host must update the settings in register [Table 187, Register 0x11F](#) [0], [Table 188, Register 0x120](#) [7:2] and [Table 184, Register 0x11C](#) [5:4] first prior to updating the settings in the register [Table 187, Register 0x11F](#) [7:1].

NOTE 3 This register is only applicable if [Table 247, Register 0x4F](#) [6] = '0'. For any other setting in [Table 247, Register 0x4F](#) [6], this register does not apply and it is a don't care.

NOTE 4 The setting for the Over Voltage must be higher than Power Good High Side Voltage threshold in [Table 188, Register 0x120](#)[7:6].

NOTE 5 This is the time it takes for buck regulator to go from steady state voltage to 0 V.

11.4.6 Miscellaneous Registers (cont'd)

Table 189 — Register 0x121

| R121 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7:6 | RW | 10 | R121 [7:6]: SWE_MODE_SELECT Switch Node E Output Regulator Mode Selection ^[3] 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode) |
| 5:4 | RW | 01 | R121 [5:4]: SWE_SWITCHING_FREQ Switch Node E Output Regulator Switching Frequency ^[3] 00 = 500 KHz 01 = 750 KHz 10 = Reserved 11 = Reserved |
| 3:2 | RW | 10 | R121 [3:2]: SWF_MODE_SELECT Switch Node F Output Regulator Mode Selection ^[4] 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode) |
| 1:0 | RW | 01 | R121 [1:0]: SWF_SWITCHING_FREQ Switch Node F Output Regulator Switching Frequency ^[4] 00 = 500 KHz 01 = 750 KHz 10 = Reserved 11 = Reserved |

- NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 255, Register 0x57](#).
- NOTE 2 If required, the host must adjust this register first before issuing VR Enable command in [Table 155, Register 0x32](#) [7].
- NOTE 3 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00' or '01'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.
- NOTE 4 This register is only applicable if [Table 247, Register 0x4F](#) [6] = '0'. For any other setting in [Table 247, Register 0x4F](#) [6], this register does not apply and it is a don't care.

11.4.6 Miscellaneous Registers (cont'd)

Table 190 — Register 0x122

| R122 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7:5 | RW | 001 | R122 [7:5]: SWE_OUTPUT_SOFT_START_TIME SWE Output Regulator Soft Start Time After VR Enable ^{[3],[4]} 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms ... 111 = 14 ms |
| 4 | RV | 0 | R122 [4]: Reserved |
| 3:1 | RW | 001 | R122 [3:1]: SWF_OUTPUT_SOFT_START_TIME SWF Output Regulator Soft Start Time After VR Enable ^{[4],[5]} 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms ... 111 = 14 ms |
| 0 | RV | 0 | R122 [0]: Reserved |

- NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 264, Register 0x60](#).
- NOTE 2 If required, the host must adjust this register first before issuing VR Enable command in [Table 155, Register 0x32 \[7\]](#).
- NOTE 3 This register is only applicable if [Table 247, Register 0x4F \[5,0\]](#) = '00' or '01'. For any other setting in [Table 247, Register 0x4F \[5,0\]](#), this register does not apply and it is a don't care.
- NOTE 4 This is the time it takes for buck regulator to go from 0 V to steady state voltage (the actual voltage varies based on pre-programmed voltage).
- NOTE 5 This register is only applicable if [Table 247, Register 0x4F \[6\]](#) = '0'. For any other setting in [Table 247, Register 0x4F \[6\]](#), this register does not apply and it is a don't care.

11.4.6 Miscellaneous Registers (cont'd)

Table 191 — Register 0x123

| R123 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description |
| 7:2 | RV | 0 | R123 [7:2]: Reserved |
| 1 | RW | 0 | R123 [1]: SWE_REGULATOR_CONTROL Disable SWE Regulator Output ^{[1],[2],[3]} 0 = Disable Switch Node E Output Regulator 1 = Enable Switch Node E Output Regulator |
| 0 | RW | 0 | R123 [0]: SWF_REGULATOR_CONTROL Disable SWF Regulator Output ^{[2],[3],[4]} 0 = Disable Switch Node F Output Regulator 1 = Enable Switch Node F Output Regulator |

NOTE 1 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00' or '01'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 2 This bit must be used only after power up sequence (after VR Enable command). At first power up, PMIC automatically updates the status of this register to '1' after VR Enable command. When VR Enable command is registered, the PMIC updates this register based on Power On Sequence Configuration (0 to 5) setting. If enabled in Power On Sequence Configuration 0 to 5 registers, only then, under non write-protect mode of operation, the PMIC's output regulator can be disabled by clearing this bit and they can be re-enabled again by setting this bit. The PMIC does not alter its Power Good output signal and keeps it asserted High. If any regulator is not enabled in Power on Sequence Configuration 0 to 5, it cannot be enabled using this register. For example, if only SWA is enabled and SWB, SWC, SWD, SWE, and SWF is not enabled in [Table 232, Register 0x40](#) [7:0] to [Table 236, Register 0x44](#) [7:0], [Table 265, Register 0x61](#) [7:0] then only SWA can be disabled and then re-enabled again but SWB, SWC, SWD, SWE and SWF cannot be enabled using [Table 152, Register 0x2F](#) [6:3], [Table 191, Register 0x123](#) [1:0].

NOTE 3 In non write-protect mode, after VR enable command, if any output regulators are disabled by clearing [Table 152, Register 0x2F](#) [6:3], [Table 191, Register 0x123](#) [1:0] and then if host issues VR Disable command or PMIC internally triggers VR Disable command, the PMIC keeps the disabled output regulator in [Table 152, Register 0x2F](#) [6:3], [Table 191, Register 0x123](#) [1:0] off and remaining output regulators are disabled by following the Power Off Sequence Configuration 0 to 5 settings.

NOTE 4 This register is only applicable if [Table 247, Register 0x4F](#) [6] = '0'. For any other setting in [Table 247, Register 0x4F](#) [6], this register does not apply and it is a don't care.

Table 192 — Register 0x12E

| R12E | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description |
| 7:6 | RW | 0 | R12E [7:6]: RESET_N_CONTROL Reset_n Input Pin Enable & Configuration Control 00 = Disable Reset_n Input Pin 01 = Enable; Reset_n assertion resets only Bus Interface (i.e., I ² C and I ³ C bus) ^[1] All other encodings are reserved |
| 5:0 | RV | 0 | R12E [5:0] Reserved |

NOTE 1 The PMIC resets I²C/I³C interface as if it was a power on reset. The PMIC returns to I²C mode ([Table 155, Register 0x32](#) [6] = '0'), 1 byte address mode ([Table 153, Register 0x30](#) [2] = '0'), clears [Table 115, Register 0x0A](#) [3:2] = '00', [Table 158, Register 0x34](#) [7:5] = '000' and [Table 158, Register 0x34](#) [3:1] = '111'. The host shall re-issue SETHID followed by SETAASA CCC to ensure all components on the module are aligned to same mode of operation. Further, the host should also update the [Table 153, Register 0x30](#) [2] to '1' for 2 byte address mode.

11.4.6 Miscellaneous Registers (cont'd)

Table 193 — Register 0x12F

| R12F | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description ^{[1],[2],[3]} |
| 7:6 | RV | 0 | R12F [7:6]: Reserved |
| 5:4 | RW | 0 | R12F [5:4]: ERROR_INJECTION_RAIL_SELECTION_EXT Error Injection - Output Rail Selection Extension ^{[4],[5]} 00 = Undefined 01 = SWE Output Only 10 = SWF Output Only 11 = Reserved |
| 3:2 | RV | 0 | R12F [3:2]: Reserved |
| 1:0 | RW | 0 | R12F [1:0]: ERROR_INJECTION_MTP_SELECTION Error Injection - MTP Selection ^[6] 00 = Undefined 01 = DIMM Vendor MTP 10 = PMIC Vendor MTP 11 = Reserved |

- NOTE 1 Refer to Clause 6.28 for error function usage model. The host can erase the error log registers ([Table 109, Register 0x04](#) to [Table 112, Register 0x07](#)) by writing 0x74 to [Table 162, Register 0x39](#).
- NOTE 2 To exit from Error Injection Mode, the PMIC must go through power cycle of both VIN_Bulk and VIN_Mgmt input supply.
- NOTE 3 Error injection function utilizes two registers: [Table 159, Register 0x35](#) and [Table 193, Register 0x12F](#).
- NOTE 4 The register [Table 159, Register 0x35](#) [6:4] and [Table 193, Register 0x12F](#) [5:4] is only applicable if [Table 159, Register 0x35](#) [2:0] is '000' and [Table 193, Register 0x12F](#) [1:0] = '00'. Any value other than '000' in [Table 159, Register 0x35](#) [6:4], '00' in [Table 193, Register 0x12F](#) [5:4], '000' in [Table 159, Register 0x35](#) [2:0] and '00' in [Table 193, Register 0x12F](#) [1:0] is considered an illegal setting and PMIC operation is not guaranteed.
- NOTE 5 If dual or three phase regulator is selected for SWA, SWB and SWE, use SWA encoding to inject the error. If dual phase regulator is selected for SWC and SWF, use SWC encoding to inject the error. Register [Table 159, Register 0x35](#) [3] selects either over voltage or under voltage condition for the setting selected in this register.
- NOTE 6 This register [Table 193, Register 0x12F](#) [1:0] is only applicable if [Table 159, Register 0x35](#) [6:0] is '000 0000' and [Table 193, Register 0x12F](#) [5:4] is '00'. Any value other than '000 0000' in [Table 159, Register 0x35](#) [6:0] and '00' in [Table 193, Register 0x12F](#) [5:4] is considered an illegal setting and PMIC operation is not guaranteed.

Table 194 — Register 0x130

| R130 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description |
| 7:0 | ROA | - | R130 [7:0]: SERIAL_NUMBER_BYTE_0 Byte 0 of the Unique 56-bit Serial number Serial number is vendor specific |

11.4.6 Miscellaneous Registers (cont'd)

Table 195 — Register 0x131

| R131 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description |
| 7:0 | ROA | - | R131 [7:0]: SERIAL_NUMBER_BYTE_1 Byte 1 of the Unique 56-bit Serial number Serial number is vendor specific |

Table 196 — Register 0x132

| R132 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description |
| 7:0 | ROA | - | R132 [7:0]: SERIAL_NUMBER_BYTE_2 Byte 2 of the Unique 56-bit Serial number Serial number is vendor specific |

Table 197 — Register 0x133

| R133 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description |
| 7:0 | ROA | - | R133 [7:0]: SERIAL_NUMBER_BYTE_3 Byte 3 of the Unique 56-bit Serial number Serial number is vendor specific |

Table 198 — Register 0x134

| R134 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description |
| 7:0 | ROA | - | R134 [7:0]: SERIAL_NUMBER_BYTE_4 Byte 4 of the Unique 56-bit Serial number Serial number is vendor specific |

Table 199 — Register 0x135

| R135 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description |
| 7:0 | ROA | - | R135 [7:0]: SERIAL_NUMBER_BYTE_5 Byte 5 of the Unique 56-bit Serial number Serial number is vendor specific |

11.4.6 Miscellaneous Registers (cont'd)

Table 200 — Register 0x136

| R136 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description |
| 7:0 | ROA | - | R136 [7:0]: SERIAL_NUMBER_BYTE_6 Byte 6 of the Unique 56-bit Serial number Serial number is vendor specific |

Table 201 — Register 0x140

| R140 - 1st Fault Error Log | | | |
|----------------------------|-----------|---------|--|
| Bits | Attribute | Default | Description |
| 7 | RON | 0 | R140 [7]: SWA_OV_FAULT SWA Buck Regulator OV Fault 0 = No Fault 1 = Fault |
| 6 | RON | 0 | R140 [6]: SWB_OV_FAULT SWB Buck Regulator OV Fault 0 = No Fault 1 = Fault |
| 5 | RON | 0 | R140 [5]: SWC_OV_FAULT SWC Buck Regulator OV Fault 0 = No Fault 1 = Fault |
| 4 | RON | 0 | R140 [4]: SWD_OV_FAULT SWD Buck Regulator OV Fault 0 = No Fault 1 = Fault |
| 3 | RON | 0 | R140 [3]: SWE_OV_FAULT SWE Buck Regulator OV Fault 0 = No Fault 1 = Fault |
| 2 | RON | 0 | R140 [2]: SWF_OV_FAULT SWF Buck Regulator OV Fault 0 = No Fault 1 = Fault |
| 1 | RON | 0 | R140 [1]: VIN_BULK_OV_FAULT VIN_Bulk OV Fault 0 = No Fault 1 = Fault |
| 0 | RV | 0 | R140 [0]: Reserved |

11.4.6 Miscellaneous Registers (cont'd)**Table 202 — Register 0x141**

| R141 - 1st Fault Error Log | | | |
|-----------------------------------|------------------|----------------|--|
| Bits | Attribute | Default | Description |
| 7 | RON | 0 | R141 [7]: SWA_UV_FAULT SWA Buck Regulator UV Fault 0 = No Fault 1 = Fault |
| 6 | RON | 0 | R141 [6]: SWB_UV_FAULT SWB Buck Regulator UV Fault 0 = No Fault 1 = Fault |
| 5 | RON | 0 | R141 [5]: SWC_UV_FAULT SWC Buck Regulator UV Fault 0 = No Fault 1 = Fault |
| 4 | RON | 0 | R141 [4]: SWD_UV_FAULT SWD Buck Regulator UV Fault 0 = No Fault 1 = Fault |
| 3 | RON | 0 | R141 [3]: SWE_UV_FAULT SWE Buck Regulator UV Fault 0 = No Fault 1 = Fault |
| 2 | RON | 0 | R141 [2]: SWF_UV_FAULT SWF Buck Regulator UV Fault 0 = No Fault 1 = Fault |
| 1 | RV | 0 | R141 [1]: Reserved |
| 0 | RON | 0 | R141 [0]: CRITICAL_TEMP_FAULT Critical Temperature Fault 0 = No Fault 1 = Fault |

Table 203 — Register 0x142

| R142 - 2nd Fault Error Log | | | |
|-----------------------------------|------------------|----------------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 140[7:0] |

11.4.6 Miscellaneous Registers (cont'd)

Table 204 — Register 0x143

| R143 - 2nd Fault Error Log | | | |
|----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 141[7:0] |

Table 205 — Register 0x144

| R144 - 3rd Fault Error Log | | | |
|----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 140[7:0] |

Table 206 — Register 0x145

| R145 - 3rd Fault Error Log | | | |
|----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 141[7:0] |

Table 207 — Register 0x146

| R146 - 4th Fault Error Log | | | |
|----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 140[7:0] |

Table 208 — Register 0x147

| R147 - 4th Fault Error Log | | | |
|----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 141[7:0] |

Table 209 — Register 0x148

| R148 - 5th Fault Error Log | | | |
|----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 140[7:0] |

11.4.6 Miscellaneous Registers (cont'd)

Table 210 — Register 0x149

| R149 - 5th Fault Error Log | | | |
|----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 141[7:0] |

Table 211 — Register 0x14A

| R14A - 6th Fault Error Log | | | |
|----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 140[7:0] |

Table 212 — Register 0x14B

| R14B - 6th Fault Error Log | | | |
|----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 141[7:0] |

Table 213 — Register 0x14C

| R14C - 7th Fault Error Log | | | |
|----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 140[7:0] |

Table 214 — Register 0x14D

| R14D - 7th Fault Error Log | | | |
|----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 141[7:0] |

Table 215 — Register 0x14E

| R14E - 8th Fault Error Log | | | |
|----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 140[7:0] |

11.4.6 Miscellaneous Registers (cont'd)

Table 216 — Register 0x14F

| R14F - 8th Fault Error Log | | | |
|----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 141[7:0] |

Table 217 — Register 0x150

| R150 - 9th Fault Error Log | | | |
|----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 140[7:0] |

Table 218 — Register 0x151

| R151 - 9th Fault Error Log | | | |
|----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 141[7:0] |

Table 219 — Register 0x152

| R152 - 10th Fault Error Log | | | |
|-----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 140[7:0] |

Table 220 — Register 0x153

| R153 - 10th Fault Error Log | | | |
|-----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 141[7:0] |

Table 221 — Register 0x154

| R154 - 11th Fault Error Log | | | |
|-----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 140[7:0] |

11.4.6 Miscellaneous Registers (cont'd)

Table 222 — Register 0x155

| R155 - 11th Fault Error Log | | | |
|-----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 141[7:0] |

Table 223 — Register 0x156

| R156 - 12th Fault Error Log | | | |
|-----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 140[7:0] |

Table 224 — Register 0x157

| R157 - 12th Fault Error Log | | | |
|-----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 141[7:0] |

Table 225 — Register 0x158

| R158 - 13th Fault Error Log | | | |
|-----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 140[7:0] |

Table 226 — Register 0x159

| R159 - 13th Fault Error Log | | | |
|-----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 141[7:0] |

Table 227 — Register 0x15A

| R15A - 14th Fault Error Log | | | |
|-----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 140[7:0] |

11.4.6 Miscellaneous Registers (cont'd)

Table 228 — Register 0x15B

| R15B - 14th Fault Error Log | | | |
|-----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 141[7:0] |

Table 229 — Register 0x15C

| R15C - 15th Fault Error Log | | | |
|-----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 140[7:0] |

Table 230 — Register 0x15D

| R15D - 15th Fault Error Log | | | |
|-----------------------------|-----------|---------|-------------------------------------|
| Bits | Attribute | Default | Description |
| 7:0 | RON | 0 | See encoding definition in 141[7:0] |

11.5 DIMM Vendor Region Register Map

Table 231 — DIMM Vendor Region - Register Map

| Register | Attribute | Description |
|--------------------------|-----------|---|
| Table 232, Register 0x40 | RWPE | R40 [7:0] Power On Sequence Config 0 |
| Table 233, Register 0x41 | RWPE | R41 [7:0] Power On Sequence Config 1 |
| Table 234, Register 0x42 | RWPE | R42 [7:0] Power On Sequence Config 2 |
| Table 235, Register 0x43 | RWPE | R43 [7:0] Power On Sequence Config 3 |
| Table 236, Register 0x44 | RWPE | R44 [7:0] Power On Sequence Config 4 |
| Table 237, Register 0x45 | RWPE | R45 [7:1] SWA Voltage Setting R45 [0] SWA Power Good Low Side Threshold |
| Table 238, Register 0x46 | RWPE | R46 [7:6] SWA Power Good High Side Threshold R46 [5:4] SWA Over Voltage Threshold R46 [3:2] SWA Under Voltage Lockout Threshold R46 [1:0] SWA Soft Stop Time |
| Table 239, Register 0x47 | RWPE | R47 [7:1] SWB Voltage Setting R47 [0] SWB Power Good Low Side Threshold |
| Table 240, Register 0x48 | RWPE | R48 [7:6] SWB Power Good High Side Threshold R48 [5:4] SWB Over Voltage Threshold R48 [3:2] SWB Under Voltage Lockout Threshold R48 [1:0] SWB Soft Stop Time |
| Table 241, Register 0x49 | RWPE | R49 [7:1] SWC Voltage Setting R49 [0] SWC Power Good Low Side Threshold |
| Table 242, Register 0x4A | RWPE | R4A [7:6] SWC Power Good High Side Threshold R4A [5:4] SWC Over Voltage Threshold R4A [3:2] SWC Under Voltage Lockout Threshold R4A [1:0] SWC Soft Stop Time |
| Table 243, Register 0x4B | RWPE | R4B [7:1] SWD Voltage Setting R4B [0] SWD Power Good Low Side Threshold |
| Table 244, Register 0x4C | RWPE | R4C [7:6] SWD Power Good High Side Threshold R4C [5:4] SWD Over Voltage Threshold R4C [3:2] SWD Under Voltage Lockout Threshold R4C [1:0] SWD Soft Stop Time |
| Table 245, Register 0x4D | RWPE | R4D [7:6] SWA Mode Select R4D [5:4] SWA Switching Frequency R4D [3:2] SWB Mode Select R4D [1:0] SWB Switching Frequency |
| Table 246, Register 0x4E | RWPE | R4E [7:6] SWC Mode Select R4E [5:4] SWC Switching Frequency R4E [3:2] SWD Mode Select R4E [1:0] SWD Switching Frequency |

Table 231 — DIMM Vendor Region - Register Map (cont'd)

| Register | Attribute | Description |
|--------------------------|-----------|--|
| Table 247, Register 0x4F | RWPE | R4F [7] Reserved R4F [6] SWC, SWF Single or Dual Phase Regulator Select R4F [5] SWA, SWB, SWE Three Phase Regulator Select Enable R4F [4:1] Reserved R4F [0] SWA, SWB Single or Dual Phase Regulator Select |
| Table 248, Register 0x50 | RWPE | R50 [7:6] SWA Output Current Limiter Warning Threshold R50 [5:4] SWB Output Current Limiter Warning Threshold R50 [3:2] SWC Output Current Limiter Warning Threshold R50 [1:0] SWD Output Current Limiter Warning Threshold |
| Table 249, Register 0x51 | RWPE | R51 [7:6] VOUT_1.8V LDO Setting R51 [5:3] Output Voltage Range Selection for SWA, SWB and SWC R51 [2:1] VOUT_1.0V LDO Setting R51 [0] Output Voltage Range Selection for SWD |
| Table 250, Register 0x52 | RWPE | R52 [7:6] SWE Output Current Limiter Warning Threshold R52 [5:4] SWF Output Current Limiter Warning Threshold R52 [3:1] Output Voltage Range Selection for SWE and SWF R52 [0] Output Voltage Range Selection SWC Extension |
| Table 251, Register 0x53 | RWPE | R53 [7:1] SWE Voltage Setting R53 [0] SWE Power Good Low Side Threshold |
| Table 252, Register 0x54 | RWPE | R54 [7:6] SWE Power Good High Side Threshold R54 [5:4] SWE Over Voltage Threshold R54 [3:2] SWE Under Voltage Lockout Threshold R54 [1:0] SWE Soft Stop Time |
| Table 253, Register 0x55 | RWPE | R55 [7:1] SWF Voltage Setting R55 [0] SWF Power Good Low Side Threshold |
| Table 254, Register 0x56 | RWPE | R56 [7:6] SWF Power Good High Side Threshold R56 [5:4] SWF Over Voltage Threshold R56 [3:2] SWF Under Voltage Lockout Threshold R56 [1:0] SWF Soft Stop Time |
| Table 255, Register 0x57 | RWPE | R57 [7:6] SWE Mode Select R57 [5:4] SWE Switching Frequency R57 [3:2] SWF Mode Select R57 [1:0] SWF Switching Frequency |
| Table 256, Register 0x58 | RWPE | R58 [7:0] Power Off Sequence Config 0 |
| Table 257, Register 0x59 | RWPE | R59 [7:0] Power Off Sequence Config 1 |
| Table 258, Register 0x5A | RWPE | R5A [7:0] Power Off Sequence Config 2 |
| Table 259, Register 0x5B | RWPE | R5B [7:0] Power Off Sequence Config 3 |
| Table 260, Register 0x5C | RWPE | R5C [7:0] Power Off Sequence Config 4 |
| Table 261, Register 0x5D | RWPE | R5D [7:5] SWA Soft Start Time R5D [4] Reserved R5D [3:1] SWB Soft Start Time R5D [0] Reserved |

Table 231 — DIMM Vendor Region - Register Map (cont'd)

| Register | Attribute | Description |
|--------------------------|-----------|--|
| Table 262, Register 0x5E | RWPE | R5E [7:5] SWC Soft Start Time R5E [4] Reserved R5E [3:1] SWD Soft Start Time R5E [0] Reserved |
| Table 263, Register 0x5F | RWPE | R5F [7] R2F [2] CONTROL R5F [6] PMIC Auto Power On Enable R5F [5] VR_OE Pin Enable R5F [4] R32 [4] Control R5F [3:0] Reserved |
| Table 264, Register 0x60 | RWPE | R60 [7:5] SWE Soft Start Time R60 [4] Reserved R60 [3:1] SWF Soft Start Time R60 [0] Reserved |
| Table 265, Register 0x61 | RWPE | R61 [7:0] Power On Sequence Config 5 |
| Table 266, Register 0x62 | RWPE | R62 [7:0] Power Off Sequence Config 5 |
| Table 267, Register 0x63 | RWPE | R63 [7:6] Power On Sequence Config 0 Extension R63 [5:4] Power On Sequence Config 1 Extension R63 [3:2] Power On Sequence Config 2 Extension R63 [1:0] Power On Sequence Config 3 Extension |
| Table 268, Register 0x64 | RWPE | R64 [7:6] Power On Sequence Config 4 Extension R64 [5:4] Power On Sequence Config 5 Extension R64 [3:0] Reserved |
| Table 269, Register 0x65 | RWPE | R65 [7:6] Power Off Sequence Config 0 Extension R65 [5:4] Power Off Sequence Config 1 Extension R65 [3:2] Power Off Sequence Config 2 Extension R65 [1:0] Power Off Sequence Config 3 Extension |
| Table 270, Register 0x66 | RWPE | R66 [7:6] Power Off Sequence Config 4 Extension R66 [5:4] Power Off Sequence Config 5 Extension R66 [3:0] Reserved |
| Table 271, Register 0x67 | RWPE | R67 [7:0] SWA Output High Current Consumption Warning Threshold |
| Table 272, Register 0x68 | RWPE | R68 [7:0] SWB Output High Current Consumption Warning Threshold |
| Table 273, Register 0x69 | RWPE | R69 [7:0] SWC Output High Current Consumption Warning Threshold |
| Table 274, Register 0x6A | RWPE | R6A [7:0] SWD Output High Current Consumption Warning Threshold |
| Table 275, Register 0x6B | RWPE | R6B [7:0] SWE Output High Current Consumption Warning Threshold |
| Table 276, Register 0x6C | RWPE | R6C [7:0] SWF Output High Current Consumption Warning Threshold |
| 0x6D to 0x6E | RV | Reserved |
| Table 277, Register 0x6F | RWPE | R6F [7:0] DIMM Vendor Region 8 bit CRC |

11.6 DIMM Vendor Region Register Definition

Table 232 — Register 0x40

| R40 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description ^[1] |
| 7 | RWPE | 0 | R40 [7]: POWER_ON_SEQUENCE_CONFIG0 PMIC Power On Sequence Config 0 ^{[2],[3]} 0 = Do Not Execute Config 0 1 = Execute Config 0 |
| 6 | RWPE | 0 | R40 [6]: POWER_ON_SEQUENCE_CONFIG0_SWA_ENABLE Enable SWA Output Regulator. 0 = No action 1 = Enable SWA Output Regulator |
| 5 | RWPE | 0 | R40 [5]: POWER_ON_SEQUENCE_CONFIG0_SWB_ENABLE Enable SWB Output Regulator. ^[4] 0 = No action 1 = Enable SWB Output Regulator |
| 4 | RWPE | 0 | R40 [4]: POWER_ON_SEQUENCE_CONFIG0_SWC_ENABLE Enable SWC Output Regulator. 0 = No action 1 = Enable SWC Output Regulator |
| 3 | RWPE | 0 | R40 [3]: POWER_ON_SEQUENCE_CONFIG0_SWD_ENABLE Enable SWD Output Regulator. 0 = No action 1 = Enable SWD Output Regulator |
| 2:0 | RWPE | 001 | R40 [2:0]: POWER_ON_SEQUENCE_CONFIG0_IDLE Idle time after Power On Sequence Config 0 ^[5] 000 = 0 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms 100 = 8 ms 101 = 10 ms 110 = 12 ms 111 = 24 ms |

NOTE 1 The PMIC always starts with power on sequence configuration 0 register and executes remaining power on sequence configuration registers (1 to 5) in sequential order.

NOTE 2 Power on sequence configuration 0 is total of 10 bit register. 8 bits as shown in [Table 232, Register 0x40 \[7:0\]](#) plus 2 bits in [Table 267, Register 0x63 \[7:6\]](#).

NOTE 3 If bit [7] = '0', bits [6:0] and [Table 267, Register 0x63 \[7:6\]](#) are ignored and PMIC moves to next power on sequence configuration register. If bit [7] = '1', PMIC executes bits [6:0] and [Table 267, Register 0x63 \[7:6\]](#) as configured; if no new rail is turned on, the PMIC simply waits the idle time as configured and then moves to next power sequence configuration register.

NOTE 4 This register is only applicable if [Table 247, Register 0x4F \[5,0\]](#) = '00'. For any other setting in [Table 247, Register 0x4F \[5,0\]](#), this register does not apply and it is a don't care.

NOTE 5 Idle time is the additional time after soft-start time expires. The PMIC waits sum of Soft Start time and Idle time before it executes the next power on sequence configuration register. If more than one regulators are enabled, the PMIC uses the largest value of the soft start time among the regulators that are enabled in this configuration register.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 233 — Register 0x41

| R41 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7 | RWPE | 0 | R41 [7]: POWER_ON_SEQUENCE_CONFIG1 PMIC Power On Sequence Config 1 0 = Do Not Execute Config ^[3] 1 1 = Execute Config 1 |
| 6 | RWPE | 0 | R41 [6]: POWER_ON_SEQUENCE_CONFIG1_SWA_ENABLE Enable SWA Output Regulator. 0 = No action 1 = Enable SWA Output Regulator |
| 5 | RWPE | 0 | R41 [5]: POWER_ON_SEQUENCE_CONFIG1_SWB_ENABLE Enable SWB Output Regulator. ^[4] 0 = No action 1 = Enable SWB Output Regulator |
| 4 | RWPE | 0 | R41 [4]: POWER_ON_SEQUENCE_CONFIG1_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = No action 1 = Enable SWC Output Regulator |
| 3 | RWPE | 0 | R41 [3]: POWER_ON_SEQUENCE_CONFIG1_SWD_ENABLE Enable Switch Node D Output Regulator. 0 = No action 1 = Enable SWD Output Regulator |
| 2:0 | RWPE | 001 | R41 [2:0]: POWER_ON_SEQUENCE_CONFIG1_IDLE Idle time after Power On Sequence Config 1 ^[5] 000 = 0 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms 100 = 8 ms 101 = 10 ms 110 = 12 ms 111 = 24 ms |

NOTE 1 The PMIC always starts with power on sequence configuration 0 register and executes remaining power on sequence configuration registers (1 to 5) in sequential order.

NOTE 2 Power on sequence configuration 1 is total of 10 bit register. 8 bits as shown in [Table 233, Register 0x41 \[7:0\]](#) plus 2 bits in [Table 267, Register 0x63 \[5:4\]](#).

NOTE 3 If bit [7] = '0', bits [6:0] and [Table 267, Register 0x63 \[5:4\]](#) are ignored and PMIC moves to next power on sequence configuration register. If bit [7] = '1', PMIC executes bits [6:0] and [Table 267, Register 0x63 \[5:4\]](#) as configured; if no new rail is turned on, the PMIC simply waits the idle time as configured and then moves to next power sequence configuration register.

NOTE 4 This register is only applicable if [Table 247, Register 0x4F \[5,0\]](#) = '00'. For any other setting in [Table 247, Register 0x4F \[5,0\]](#), this register does not apply and it is a don't care.

NOTE 5 Idle time is the additional time after soft-start time expires. The PMIC waits sum of Soft Start time and Idle time before it executes the next power on sequence configuration register. If more than one regulators are enabled, the PMIC uses the largest value of the soft start time among the regulators that are enabled in this configuration register.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 234 — Register 0x42

| R42 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7 | RWPE | 0 | R42 [7]: POWER_ON_SEQUENCE_CONFIG2 PMIC Power On Sequence Config 2 ^[3] 0 = Do Not Execute Config 2 1 = Execute Config 2 |
| 6 | RWPE | 0 | R42 [6]: POWER_ON_SEQUENCE_CONFIG2_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = No action 1 = Enable Switch Node A Output Regulator |
| 5 | RWPE | 0 | R42 [5]: POWER_ON_SEQUENCE_CONFIG2_SWB_ENABLE Enable Switch Node B Output Regulator. ^[4] 0 = No action 1 = Enable Switch Node B Output Regulator |
| 4 | RWPE | 0 | R42 [4]: POWER_ON_SEQUENCE_CONFIG2_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = No action 1 = Enable Switch Node C Output Regulator |
| 3 | RWPE | 0 | R42 [3]: POWER_ON_SEQUENCE_CONFIG2_SWD_ENABLE Enable Switch Node D Output Regulator. 0 = No action 1 = Enable Switch Node D Output Regulator |
| 2:0 | RWPE | 001 | R42 [2:0]: POWER_ON_SEQUENCE_CONFIG2_IDLE Idle time after Power On Sequence Config 2 ^[5] 000 = 0 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms 100 = 8 ms 101 = 10 ms 110 = 12 ms 111 = 24 ms |

NOTE 1 The PMIC always starts with power on sequence configuration 0 register and executes remaining power on sequence configuration registers (1 to 5) in sequential order.

NOTE 2 Power on sequence configuration 2 is total of 10 bit register. 8 bits as shown in [Table 234, Register 0x42](#) [7:0] plus 2 bits in [Table 267, Register 0x63](#) [3:2].

NOTE 3 If bit [7] = '0', bits [6:0] and [Table 267, Register 0x63](#) [3:2] are ignored and PMIC moves to next power on sequence configuration register. If bit [7] = '1', PMIC executes bits [6:0] and [Table 267, Register 0x63](#) [3:2] as configured; if no new rail is turned on, the PMIC simply waits the idle time as configured and then moves to next power sequence configuration register.

NOTE 4 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 5 Idle time is the additional time after soft-start time expires. The PMIC waits sum of Soft Start time and Idle time before it executes the next power on sequence configuration register. If more than one regulators are enabled, the PMIC uses the largest value of the soft start time among the regulators that are enabled in this configuration register.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 235 — Register 0x43

| R43 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7 | RWPE | 0 | R43 [7]: POWER_ON_SEQUENCE_CONFIG3 PMIC Power On Sequence Config 3 0 = Do Not Execute Config 3 ^[3] 1 = Execute Config 3 |
| 6 | RWPE | 0 | R43 [6]: POWER_ON_SEQUENCE_CONFIG3_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = No Action 1 = Enable Switch Node A Output Regulator |
| 5 | RWPE | 0 | R43 [5]: POWER_ON_SEQUENCE_CONFIG3_SWB_ENABLE Enable Switch Node B Output Regulator. ^[4] 0 = No Action 1 = Enable Switch Node B Output Regulator |
| 4 | RWPE | 0 | R43 [4]: POWER_ON_SEQUENCE_CONFIG3_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = No Action 1 = Enable Switch Node C Output Regulator |
| 3 | RWPE | 0 | R43 [3]: POWER_ON_SEQUENCE_CONFIG3_SWD_ENABLE Enable Switch Node D Output Regulator. 0 = No Action 1 = Enable Switch Node D Output Regulator |
| 2:0 | RWPE | 001 | R43 [2:0]: POWER_ON_SEQUENCE_CONFIG3_IDLE Idle time after Power On Sequence Config 3 ^[5] 000 = 0 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms 100 = 8 ms 101 = 10 ms 110 = 12 ms 111 = 24 ms |

NOTE 1 The PMIC always starts with power on sequence configuration 0 register and executes remaining power on sequence configuration registers (1 to 5) in sequential order.

NOTE 2 Power on sequence configuration 3 is total of 10 bit register. 8 bits as shown in [Table 235, Register 0x43](#) [7:0] plus 2 bits in [Table 267, Register 0x63](#) [1:0].

NOTE 3 If bit [7] = '0', bits [6:0] and [Table 267, Register 0x63](#) [1:0] are ignored and PMIC moves to next power on sequence configuration register. If bit [7] = '1', PMIC executes bits [6:0] and [Table 267, Register 0x63](#) [1:0] as configured; if no new rail is turned on, the PMIC simply waits the idle time as configured and then moves to next power sequence configuration register.

NOTE 4 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 5 Idle time is the additional time after soft-start time expires. The PMIC waits sum of Soft Start time and Idle time before it executes the next event. If more than one regulators are enabled, the PMIC uses the largest value of the soft start time among the regulators that are enabled in this configuration register.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 236 — Register 0x44

| R44 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7 | RWPE | 0 | R44 [7]: POWER_ON_SEQUENCE_CONFIG4 PMIC Power On Sequence Config 4 0 = Do Not Execute Config 4 ^[3] 1 = Execute Config 4 |
| 6 | RWPE | 0 | R44 [6]: POWER_ON_SEQUENCE_CONFIG4_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = No Action 1 = Enable Switch Node A Output Regulator |
| 5 | RWPE | 0 | R44 [5]: POWER_ON_SEQUENCE_CONFIG4_SWB_ENABLE Enable Switch Node B Output Regulator. ^[4] 0 = No Action 1 = Enable Switch Node B Output Regulator |
| 4 | RWPE | 0 | R44 [4]: POWER_ON_SEQUENCE_CONFIG4_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = No Action 1 = Enable Switch Node C Output Regulator |
| 3 | RWPE | 0 | R44 [3]: POWER_ON_SEQUENCE_CONFIG4_SWD_ENABLE Enable Switch Node D Output Regulator. 0 = No Action 1 = Enable Switch Node D Output Regulator |
| 2:0 | RWPE | 001 | R44 [2:0]: POWER_ON_SEQUENCE_CONFIG4_IDLE Idle time after Power On Sequence Config 4 ^[5] 000 = 0 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms 100 = 8 ms 101 = 10 ms 110 = 12 ms 111 = 24 ms |

NOTE 1 The PMIC always starts with power on sequence configuration 0 register and executes remaining power on sequence configuration registers (1 to 5) in sequential order.

NOTE 2 Power on sequence configuration 4 is total of 10 bit register. 8 bits as shown in [Table 236, Register 0x44](#) [7:0] plus 2 bits in [Table 268, Register 0x64](#) [7:6].

NOTE 3 If bit [7] = '0', bits [6:0] and [Table 268, Register 0x64](#) [7:6] are ignored and PMIC moves to next power on sequence configuration register. If bit [7] = '1', PMIC executes bits [6:0] [Table 268, Register 0x64](#) [7:6] as configured; if no new rail is turned on, the PMIC simply waits the idle time as configured and then moves to next power sequence configuration register.

NOTE 4 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 5 Idle time is the additional time after soft-start time expires. The PMIC waits sum of Soft Start time and Idle time before it executes the next event. If more than one regulators are enabled, the PMIC uses the largest value of the soft start time among the regulators that are enabled in this configuration register.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 237 — Register 0x45

| R45 | | | |
|------|-----------|----------|---|
| Bits | Attribute | Default | Description |
| 7:1 | RWPE | 011 1100 | R45 [7:1]: SWA_VOLTAGE_SETTING SWA Output Regulator Voltage Setting ^[1] 000 0000 = 800 mV ^[2] or 600 mV ^[3] 000 0001 = 805 mV or 605 mV 000 0010 = 810 mV or 610 mV ... 011 1100 = 1100 mV or 900 mV ... 111 1101 = 1425 mV or 1225 mV 111 1110 = 1430 mV or 1230 mV 111 1111 = 1435 mV or 1235 mV |
| 0 | RWPE | 0 | R45 [0]: SWA_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING SWA Output Threshold Low Side Voltage For Power Good Status 0 = - 5% from the setting in Table 237, Register 0x45 [7:1] 1 = - 7.5% from the setting in Table 237, Register 0x45 [7:1] |

NOTE 1 PMIC guarantees efficiency spec within a range of 1050 mV to 1160 mV.

NOTE 2 [Table 249, Register 0x51](#) [5] = '0'.

NOTE 3 [Table 249, Register 0x51](#) [5] = '1'.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 238 — Register 0x46

| R46 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description |
| 7:6 | RWPE | 01 | R46 [7:6]: SWA_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold High Side Voltage For Power Good Status 00 = +5% from the setting in Table 237, Register 0x45 [7:1] 01 = +7.5% from the setting in Table 237, Register 0x45 [7:1] 10 = +10% from the setting in Table 237, Register 0x45 [7:1] 11 = Reserved |
| 5:4 | RWPE | 10 | R46 [5:4]: SWA_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Over Voltage Status ^[1] 00 = +7.5% from the setting in Table 237, Register 0x45 [7:1] 01 = +10% from the setting in Table 237, Register 0x45 [7:1] 10 = +12.5% from the setting in Table 237, Register 0x45 [7:1] 11 = Reserved |
| 3:2 | RWPE | 00 | R46 [3:2]: SWA_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Under Voltage Lockout Status 00 = -10% from the setting in Table 237, Register 0x45 [7:1] 01 = -12.5% from the setting in Table 237, Register 0x45 [7:1] 10 = Reserved 11 = Reserved |
| 1:0 | RWPE | 00 | R46 [1:0]: SWA_OUTPUT_SOFT_STOP_TIME SWA Output Regulator Soft Stop Time After VR Disable ^[2] 00 = 0.5 ms 01 = 1 ms 10 = 2 ms 11 = 4 ms |

NOTE 1 The setting for the Over Voltage must be higher than Power Good High Side Voltage threshold in [Table 238, Register 0x46](#)[7:6].

NOTE 2 This is the time it takes for buck regulator to go from steady state voltage to 0 V.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 239 — Register 0x47

| R47 | | | |
|------|-----------|----------|---|
| Bits | Attribute | Default | Description ^[1] |
| 7:1 | RWPE | 011 1100 | R47 [7:1]: SWB_VOLTAGE_SETTING SWB Output Regulator Voltage Setting ^[2] 000 0000 = 800 mV ^[3] or 600 mV ^[4] 000 0001 = 805 mV or 605 mV 000 0010 = 810 mV or 610 mV ... 011 1100 = 1100 mV or 900 mV ... 111 1101 = 1425 mV or 1225 mV 111 1110 = 1430 mV or 1230 mV 111 1111 = 1435 mV or 1235 mV |
| 0 | RWPE | 0 | R47 [0]: SWB_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING SWB Output Threshold Low Side Voltage For Power Good Status 0 = -5% from the setting in Table 239, Register 0x47 [7:1] 1 = -7.5% from the setting in Table 239, Register 0x47 [7:1] |

NOTE 1 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 2 PMIC guarantees efficiency spec within a range of 1050 mV to 1160 mV.

NOTE 3 [Table 249, Register 0x51](#) [4] = '0'.

NOTE 4 [Table 249, Register 0x51](#) [4] = '1'.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 240 — Register 0x48

| R48 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^[1] |
| 7:6 | RWPE | 01 | R48 [7:6]: SWB_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING SWB Output Threshold High Side Voltage For Power Good Status 00 = +5% from the setting in Table 239, Register 0x47 [7:1] 01 = +7.5% from the setting in Table 239, Register 0x47 [7:1] 10 = +10% from the setting in Table 239, Register 0x47 [7:1] 11 = Reserved |
| 5:4 | RWPE | 10 | R48 [5:4]: SWB_OVER_VOLTAGE_THRESHOLD_SETTING SWB Output Regulator Threshold For Over Voltage Status ^[2] 00 = +7.5% from the setting in Table 239, Register 0x47 [7:1] 01 = +10% from the setting in Table 239, Register 0x47 [7:1] 10 = +12.5% from the setting in Table 239, Register 0x47 [7:1] 11 = Reserved |
| 3:2 | RWPE | 00 | R48 [3:2]: SWB_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING SWB Output Regulator Threshold For Under Voltage Lockout Status 00 = -10% from the setting in Table 239, Register 0x47 [7:1] 01 = -12.5% from the setting in Table 239, Register 0x47 [7:1] 10 = Reserved 11 = Reserved |
| 1:0 | RWPE | 00 | R48 [1:0]: SWB_OUTPUT_SOFT_STOP_TIME SWB Output Regulator Soft Stop Time After VR Disable ^[3] 00 = 0.5 ms 01 = 1 ms 10 = 2 ms 11 = 4 ms |

NOTE 1 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 2 The setting for the Over Voltage must be higher than Power Good High Side Voltage threshold in [Table 240, Register 0x48](#) [7:6].

NOTE 3 This is the time it takes for buck regulator to go from steady state voltage to 0 V.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 241 — Register 0x49

| R49 | | | |
|------|-----------|----------|--|
| Bits | Attribute | Default | Description |
| 7:1 | RWPE | 011 1100 | R49 [7:1]: SWC_VOLTAGE_SETTING SWC Output Regulator Voltage Setting ^[1] 000 0000 = 800 mV ^[2] or 600 mV ^[3] or 400 mV ^[4] 000 0001 = 805 mV or 605 mV or 402.5 mV 000 0010 = 810 mV or 610 mV or 405 mV ... 011 1100 = 1100 mV or 900 mV or 550 mV ... 111 1101 = 1425 mV or 1225 mV or 712.5 mV 111 1110 = 1430 mV or 1230 mV or 715 mV 111 1111 = 1435 mV or 1235 mV or 717.5 mV |
| 0 | RWPE | 0 | R49 [0]: SWC_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold Low Side Voltage For Power Good Status 0 = -5% from the setting in Table 241, Register 0x49 [7:1] 1 = -7.5 from the setting in Table 241, Register 0x49 [7:1] |

NOTE 1 PMIC guarantees efficiency spec within a range of 1050 mV to 1160 mV.

NOTE 2 [Table 250, Register 0x52](#) [0] = '0' and [Table 249, Register 0x51](#) [3] = '0'; 5 mV step size.

NOTE 3 [Table 250, Register 0x52](#) [0] = '0' and [Table 249, Register 0x51](#) [3] = '1'; 5 mV step size.

NOTE 4 [Table 250, Register 0x52](#) [0] = '1' and [Table 249, Register 0x51](#) [3] = '0'; 2.5 mV step size.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 242 — Register 0x4A

| R4A | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description |
| 7:6 | RWPE | 01 | R4A [7:6]: SWC_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING SWC Output Threshold High Side Voltage For Power Good Status 00 = +5% from the setting in Table 241, Register 0x49 [7:1] 01 = +7.5% from the setting in Table 241, Register 0x49 [7:1] 10 = +10% from the setting in Table 241, Register 0x49 [7:1] 11 = Reserved |
| 5:4 | RWPE | 10 | R4A [5:4]: SWC_OVER_VOLTAGE_THRESHOLD_SETTING SWC Output Regulator Threshold For Over Voltage Status ^[1] 00 = +7.5% from the setting in Table 241, Register 0x49 [7:1] 01 = +10% from the setting in Table 241, Register 0x49 [7:1] 10 = +12.5% from the setting in Table 241, Register 0x49 [7:1] 11 = Reserved |
| 3:2 | RWPE | 00 | R4A [3:2]: SWC_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING SWC Output Regulator Threshold For Under Voltage Lockout Status 00 = -10% from the setting in Table 241, Register 0x49 [7:1] 01 = -12.5% from the setting in Table 241, Register 0x49 [7:1] 10 = Reserved 11 = Reserved |
| 1:0 | RWPE | 00 | R4A [1:0]: SWC_OUTPUT_SOFT_STOP_TIME SWC Output Regulator Soft Stop Time After VR Disable ^[2] 00 = 0.5 ms 01 = 1 ms 10 = 2 ms 11 = 4 ms |

NOTE 1 The setting for the Over Voltage must be higher than Power Good High Side Voltage threshold in [Table 242, Register 0x4A](#)[7:6].

NOTE 2 This is the time it takes for buck regulator to go from steady state voltage to 0 V.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 243 — Register 0x4B

| R4B | | | |
|------|-----------|----------|--|
| Bits | Attribute | Default | Description |
| 7:1 | RWPE | 011 1100 | R4B [7:1]: SWD_VOLTAGE_SETTING SWD Output Regulator Voltage Setting ^[1] 000 0000 = 1500 mV ^[2] or 2200 mV ^[3] 000 0001 = 1505 mV or 2205 mV 000 0010 = 1510 mV or 2210 mV ... 011 1100 = 1800 mV or 2500 mV ... 111 1101 = 2125 mV or 2825 mV 111 1110 = 2130 mV or 2830 mV 111 1111 = 2135 mV or 2835 mV |
| 0 | RWPE | 0 | R4B [0]: SWD_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING SWD Output Threshold Low Side Voltage For Power Good Status 0 = -5% from the setting in Table 243, Register 0x4B [7:1] 1 = -7.5% from the setting in Table 243, Register 0x4B [7:1] |

NOTE 1 PMIC guarantees efficiency spec within a range of 1750 mV to 1850 mV.

NOTE 2 [Table 249, Register 0x51 \[0\]](#) = '0'.

NOTE 3 [Table 249, Register 0x51 \[0\]](#) = '1'.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 244 — Register 0x4C

| R4C | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description |
| 7:6 | RWPE | 01 | R4C [7:6]: SWD_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING SWD Output Threshold High Side Voltage For Power Good Status 00 = +5% from the setting in Table 243, Register 0x4B [7:1] 01 = +7.5% from the setting in Table 243, Register 0x4B [7:1] 10 = Reserved 11 = Reserved |
| 5:4 | RWPE | 10 | R4C [5:4]: SWD_OVER_VOLTAGE_THRESHOLD_SETTING SWD Output Regulator Threshold For Over Voltage Status ^[1] 00 = +7.5% from the setting in Table 243, Register 0x4B [7:1] 01 = +10% from the setting in Table 243, Register 0x4B [7:1] 10 = +12.5% from the setting in Table 243, Register 0x4B [7:1] 11 = Reserved |
| 3:2 | RWPE | 00 | R4C [3:2]: SWD_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING SWD Output Regulator Threshold For Under Voltage Lockout Status 00 = -10% from the setting in Table 243, Register 0x4B [7:1] 01 = -12.5% from the setting in Table 243, Register 0x4B [7:1] 10 = Reserved 11 = Reserved |
| 1:0 | RWPE | 00 | R4C [1:0]: SWD_OUTPUT_SOFT_STOP_TIME SWD Output Regulator Soft Stop Time After VR Disable ^[2] 00 = 1 ms 01 = 2 ms 10 = 4 ms 11 = 8 ms |

NOTE 1 The setting for the Over Voltage must be higher than Power Good High Side Voltage threshold in [Table 244, Register 0x4C\[7:6\]](#).

NOTE 2 This is the time it takes for buck regulator to go from steady state voltage to 0 V.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 245 — Register 0x4D

| R4D | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description |
| 7:6 | RWPE | 10 | R4D [7:6]: SWA_MODE_SELECT Switch Node A Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; CCM (Constant on Time; Continuous Current Mode) |
| 5:4 | RWPE | 01 | R4D [5:4]: SWA_SWITCHING_FREQ Switch Node A Output Regulator Switching Frequency 00 = 500 KHz 01 = 750 KHz 10 = Reserved 11 = Reserved |
| 3:2 | RWPE | 10 | R4D [1:0]: SWB_MODE_SELECT Switch Node B Output Regulator Mode Selection ^[1] 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; CCM (Constant on Time; Continuous Current Mode) |
| 1:0 | RWPE | 01 | R4D [1:0]: SWB_SWITCHING_FREQ Switch Node B Output Regulator Switching Frequency ^[1] 00 = 500 KHz 01 = 750 KHz 10 = Reserved 11 = Reserved |

NOTE 1 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 246 — Register 0x4E

| R4E | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description |
| 7:6 | RWPE | 10 | R4E [7:6]: SWC_MODE_SELECT Switch Node C Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; CCM (Constant on Time; Continuous Current Mode) |
| 5:4 | RWPE | 01 | R4E [5:4]: SWC_SWITCHING_FREQ Switch Node C Output Regulator Switching Frequency 00 = 500 KHz 01 = 750 KHz 10 = Reserved 11 = Reserved |
| 3:2 | RWPE | 10 | R4E [3:2]: SWD_MODE_SELECT Switch Node D Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; CCM (Constant on Time; Continuous Current Mode) |
| 1:0 | RWPE | 01 | R4E [1:0]: SWD_SWITCHING_FREQ Switch Node D Output Regulator Switching Frequency 00 = Reserved 01 = 750 KHz 10 = 1000 KHz 11 = Reserved |

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 247 — Register 0x4F

| R4F | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description |
| 7 | RV | 0 | R4F [7]: Reserved |
| 6 | RWPE | 0 | R4F [6]: SWC_SWF_PHASE_MODE_SELECT SWC and SWF Phase Regulator Mode Selection 0 = Single Phase Regulator Mode (SWC, SWF) 1 = Dual Phase Regulator Mode (SWC+SWF) |
| 5 | RWPE | 0 | R4F [5]: SWA_SWB_SWE_PHASE_MODE_SELECT_MSB SWA, SWB and SWE Phase Regulator Mode Selection. When this bit is set to '1', the setting in bit [0] is a don't care & PMIC operates in a triple phase regulator mode. 00 = Single Phase Regulator Mode (SWA, SWB, SWE) 01 = Dual Phase Regulator Mode (SWA+SWB, SWE is a single phase) 1x = Three Phase Regulator Mode (SWA+SWB+SWE) |
| 4:1 | RV | 0 | R4F [4:1]: Reserved |
| 0 | RWPE | 0 | R4F [0]: SWA_SWB_PHASE_MODE_SELECT_LSB SWA and SWB Phase Regulator Mode Selection. See the description for bit [5]. 0 = Single Phase Regulator Mode (SWA, SWB) 1 = Dual Phase Regulator Mode (SWA+SWB) |

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 248 — Register 0x50

| R50 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description |
| 7:6 | RWPE | 01 | R50 [7:6]: SWA_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING PMIC5030 COT Mode, Ivalley_limit: 00 = 6A 01 = 7A 10 = 8A 11 = 9A |
| 5:4 | RWPE | 01 | R50 [5:4]: SWB_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING PMIC5030 COT Mode, Ivalley_limit ^[1] : 00 = 6A 01 = 7A 10 = 8A 11 = 9A |
| 3:2 | RWPE | 01 | R50 [3:2]: SWC_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING PMIC5030 COT Mode, Ivalley_limit: 00 = 6A 01 = 7A 10 = 8A 11 = 9A |
| 1:0 | RWPE | 01 | R50 [1:0]: SWD_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING PMIC5030 COT Mode, Ivalley_limit: 00 = 4A 01 = 4.5A 10 = 5A 11 = 5.5A |

NOTE 1 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [5,0].

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 249 — Register 0x51

| R51 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description |
| 7:6 | RWPE | 01 | R51 [7:6]: VOUT_1.8V_VOLTAGE_SETTING VOUT 1.8 V LDO Output Voltage Setting ^[1] 00 = 1.7 V 01 = 1.8 V 10 = 1.9 V 11 = Reserved |
| 5 | RWPE | 0 | R51 [5]: SWA_VOLTAGE_RANGE SWA Output Voltage Range Selection ^[2] 0 = Range: 800 mV to 1435 mV for SWA; 5 mV step size. 1 = Range: 600 mV to 1235 mV for SWA; 5 mV step size |
| 4 | RWPE | 0 | R51 [4]: SWB_VOLTAGE_RANGE SWB Output Voltage Range Selection ^{[3],[4]} 0 = Range: 800 mV to 1435 mV for SWB; 5 mV step size 1 = Range: 600 mV to 1235 mV for SWB; 5 mV step size |
| 3 | RWPE | 0 | R51 [3]: SWC_VOLTAGE_RANGE SWC Output Voltage Range Selection ^[5] . The MSB bit Table 250, Register 0x52 [0] plus this bit LSB Table 249, Register 0x51 [3] makes 2 bit encoding as following: 00 = Range: 800 mV to 1435 mV for SWC; 5 mV step size 01 = Range: 600 mV to 1235 mV for SWC; 5 mV step size 10 = Range: 400 mV to 717.5 mV for SWC; 2.5 mV step size 11 = Reserved |
| 2:1 | RWPE | 01 | R51 [2:1]: VOUT_1.0V_VOLTAGE_SETTING VOUT 1.0 V LDO Voltage Setting 00 = 0.9 V 01 = 1.0 V 10 = 1.1 V 11 = 1.2 V |
| 0 | RWPE | 0 | R51 [0]: SWD_VOLTAGE_RANGE SWD Output Voltage Range Selection ^[6] 0 = Range: 1500 mV to 2135 mV for SWD; 5 mV step size 1 = Range: 2200 mV to 2835 mV for SWD; 5 mV step size |

NOTE 1 The VOUT_1.8V Power Good threshold in register [Table 131, Register 0x1A \[2\]](#) is always fixed regardless of the setting in this register.

NOTE 2 Range selection applies to registers [Table 237, Register 0x45 \[7:1\]](#).

NOTE 3 Range selection applies to registers [Table 239, Register 0x47 \[7:1\]](#).

NOTE 4 This register is only applicable if [Table 247, Register 0x4F \[5,0\]](#) = '00'. For any other setting in [Table 247, Register 0x4F \[5,0\]](#), this register does not apply and it is a don't care.

NOTE 5 Range selection applies to registers [Table 241, Register 0x49 \[7:1\]](#).

NOTE 6 Range selection applies to registers [Table 243, Register 0x4B \[7:1\]](#).

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 250 — Register 0x52

| R52 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description |
| 7:6 | RWPE | 01 | R52 [7:6]: SWE_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING PMIC5030 COT Mode, Ivalley_limit ^[1] 00 = 6A 01 = 7A 10 = 8A 11 = 9A |
| 5:4 | RWPE | 01 | R52 [5:4]: SWF_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING PMIC5030 COT Mode, Ivalley_limit ^[2] 00 = 6A 01 = 7A 10 = 8A 11 = 9A |
| 3 | RWPE | 0 | R52 [3]: SWE_VOLTAGE_RANGE SWE Output Voltage Range Selection ^{[3],[4]} 0 = Range: 800 mV to 1435 mV for SWA; 5 mV step size. 1 = Range: 600 mV to 1235 mV for SWA; 5 mV step size |
| 2:1 | RWPE | 0 | R52 [2:1]: SWF_VOLTAGE_RANGE SWF Output Voltage Range Selection ^{[5],[6]} 00 = Range: 800 mV to 1435 mV for SWF; 5 mV step size 01 = Range: 600 mV to 1235 mV for SWF; 5 mV step size 10 = Range: 400 mV to 717.5 mV for SWF; 2.5 mV step size 11 = Reserved |
| 0 | RWPE | 0 | R52 [0]: SWC_VOLTAGE_RANGE_EXT SWC Output Voltage Range Selection ^[7] . This bit MSB plus Table 249, Register 0x51 [3] as LSB bit makes 2 bit encoding as following: 00 = Range: 800 mV to 1435 mV for SWC; 5 mV step size 01 = Range: 600 mV to 1235 mV for SWC; 5 mV step size 10 = Range: 400 mV to 717.5 mV for SWC; 2.5 mV step size 11 = Reserved |

NOTE 1 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [5,0].

NOTE 2 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [6].

NOTE 3 Range selection applies to registers [Table 251, Register 0x53](#) [7:1].

NOTE 4 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00' or '01'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 5 Range selection applies to registers [Table 253, Register 0x55](#) [7:1].

NOTE 6 This register is only applicable if [Table 247, Register 0x4F](#) [6] = '0'. For any other setting in [Table 247, Register 0x4F](#) [6], this register does not apply and it is a don't care.

NOTE 7 Range selection applies to registers [Table 241, Register 0x49](#) [7:1].

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 251 — Register 0x53

| R53 | | | |
|------|-----------|----------|---|
| Bits | Attribute | Default | Description ^[1] |
| 7:1 | RWPE | 011 1100 | R53 [7:1]: SWE_VOLTAGE_SETTING SWE Output Regulator Voltage Setting ^[2] 000 0000 = 800 mV ^[3] or 600 mV ^[4] 000 0001 = 805 mV or 605 mV 000 0010 = 810 mV or 610 mV ... 011 1100 = 1100 mV or 900 mV ... 111 1101 = 1425 mV or 1225 mV 111 1110 = 1430 mV or 1230 mV 111 1111 = 1435 mV or 1235 mV |
| 0 | RWPE | 0 | R53 [1:0]: SWE_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING SWE Output Threshold Low Side Voltage For Power Good Status 0 = - 5% from the setting in Table 251, Register 0x53 [7:1] 1 = - 7.5% from the setting in Table 251, Register 0x53 [7:1] |

NOTE 1 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00' or '01'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 2 PMIC guarantees efficiency spec within a range of 1050 mV to 1160 mV.

NOTE 3 [Table 250, Register 0x52](#) [3] = '0'.

NOTE 4 [Table 250, Register 0x52](#) [3] = '1'.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 252 — Register 0x54

| R54 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^[1] |
| 7:6 | RWPE | 01 | R54 [7:6]: SWE_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node E Output Threshold High Side Voltage For Power Good Status 00 = +5% from the setting in Table 251, Register 0x53 [7:1] 01 = +7.5% from the setting in Table 251, Register 0x53 [7:1] 10 = +10% from the setting in Table 251, Register 0x53 [7:1] 11 = Reserved |
| 5:4 | RWPE | 10 | R54 [5:4]: SWE_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node E Output Regulator Threshold For Over Voltage Status ^[2] 00 = +7.5% from the setting in Table 251, Register 0x53 [7:1] 01 = +10% from the setting in Table 251, Register 0x53 [7:1] 10 = +12.5% from the setting in Table 251, Register 0x53 [7:1] 11 = Reserved |
| 3:2 | RWPE | 00 | R54 [3:2]: SWE_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node E Output Regulator Threshold For Under Voltage Lockout Status 00 = -10% from the setting in Table 251, Register 0x53 [7:1] 01 = -12.5% from the setting in Table 251, Register 0x53 [7:1] 10 = Reserved 11 = Reserved |
| 1:0 | RWPE | 00 | R54 [1:0]: SWE_OUTPUT_SOFT_STOP_TIME SWE Output Regulator Soft Stop Time After VR Disable ^[3] 00 = 0.5 ms 01 = 1 ms 10 = 2 ms 11 = 4 ms |

NOTE 1 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00' or '01'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 2 The setting for the Over Voltage threshold must be higher than Power Good High Side Voltage threshold in [Table 252, Register 0x54](#) [7:6].

NOTE 3 This is the time it takes for buck regulator to go from steady state voltage to 0 V.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 253 — Register 0x55

| R55 | | | |
|------|-----------|----------|--|
| Bits | Attribute | Default | Description ^[1] |
| 7:1 | RWPE | 011 1100 | R55 [7:1]: SWF_VOLTAGE_SETTING SWF Output Regulator Voltage Setting ^[2] 000 0000 = 800 mV ^[3] or 600 mV ^[4] or 400 mV ^[5] 000 0001 = 805 mV or 605 mV or 402.5 mV 000 0010 = 810 mV or 610 mV or 405 mV ... 011 1100 = 1100 mV or 900 mV or 550 mV ... 111 1101 = 1425 mV or 1225 mV or 712.5 mV 111 1110 = 1430 mV or 1230 mV or 715 mV 111 1111 = 1435 mV or 1235 mV or 717.5 mV |
| 0 | RWPE | 0 | R55 [1]: SWF_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING SWF Output Threshold Low Side Voltage For Power Good Status 0 = -5% from the setting in Table 253, Register 0x55 [7:1] 1 = -7.5% from the setting in Table 253, Register 0x55 [7:1] |

NOTE 1 This register is only applicable if [Table 247, Register 0x4F](#) [6] = '0'. For any other setting in [Table 247, Register 0x4F](#) [6], this register does not apply and it is a don't care.

NOTE 2 PMIC guarantees efficiency spec within a range of 1050 mV to 1160 mV.

NOTE 3 [Table 250, Register 0x52](#) [2:1] = '00'; 5 mV step size.

NOTE 4 [Table 250, Register 0x52](#) [2:1] = '01'; 5 mV step size.

NOTE 5 [Table 250, Register 0x52](#) [2:1] = '10'; 2.5 mV step size.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 254 — Register 0x56

| R56 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^[1] |
| 7:6 | RWPE | 01 | R56 [7:6]: SWF_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING SWF Output Threshold High Side Voltage For Power Good Status 00 = +5% from the setting in Table 253, Register 0x55 [7:1] 01 = +7.5% from the setting in Table 253, Register 0x55 [7:1] 10 = +10% from the setting in Table 253, Register 0x55 [7:1] 11 = Reserved |
| 5:4 | RWPE | 10 | R56 [5:4]: SWF_OVER_VOLTAGE_THRESHOLD_SETTING SWF Output Regulator Threshold For Over Voltage Status ^[2] 00 = +7.5% from the setting in Table 253, Register 0x55 [7:1] 01 = +10% from the setting in Table 253, Register 0x55 [7:1] 10 = +12.5% from the setting in Table 253, Register 0x55 [7:1] 11 = Reserved |
| 3:2 | RWPE | 00 | R56 [3:2]: SWF_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING SWF Output Regulator Threshold For Under Voltage Lockout Status 00 = -10% from the setting in Table 253, Register 0x55 [7:1] 01 = -12.5% from the setting in Table 253, Register 0x55 [7:1] 10 = Reserved 11 = Reserved |
| 1:0 | RWPE | 00 | R56 [1:0]: SWF_OUTPUT_SOFT_STOP_TIME SWF Output Regulator Soft Stop Time After VR Disable ^[3] 00 = 0.5 ms 01 = 1 ms 10 = 2 ms 11 = 4 ms |

NOTE 1 This register is only applicable if [Table 247, Register 0x4F](#) [6] = '0'. For any other setting in [Table 247, Register 0x4F](#) [6], this register does not apply and it is a don't care.

NOTE 2 The setting for the Over Voltage must threshold be higher than Power Good High Side Voltage threshold in [Table 254, Register 0x56](#) [7:6].

NOTE 3 This is the time it takes for buck regulator to go from steady state voltage to 0 V.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 255 — Register 0x57

| R57 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description |
| 7:6 | RWPE | 10 | R57 [7:6]: SWE_MODE_SELECT Switch Node E Output Regulator Mode Selection ^[1] 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; CCM (Constant on Time; Continuous Current Mode) |
| 5:4 | RWPE | 01 | R57 [5:4]: SWE_SWITCHING_FREQ Switch Node E Output Regulator Switching Frequency ^[1] 00 = 500 KHz 01 = 750 KHz 10 = Reserved 11 = Reserved |
| 3:2 | RWPE | 10 | R57 [1:0]: SWF_MODE_SELECT Switch Node F Output Regulator Mode Selection ^[2] 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; CCM (Constant on Time; Continuous Current Mode) |
| 1:0 | RWPE | 01 | R57 [1:0]: SWF_SWITCHING_FREQ Switch Node F Output Regulator Switching Frequency ^[2] 00 = 500 KHz 01 = 750 KHz 10 = Reserved 11 = Reserved |

NOTE 1 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00' or '01'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 2 This register is only applicable if [Table 247, Register 0x4F](#) [6] = '0'. For any other setting in [Table 247, Register 0x4F](#) [6], this register does not apply and it is a don't care.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 256 — Register 0x58

| R58 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7 | RWPE | 0 | R58 [7]: POWER_OFF_SEQUENCE_CONFIG0 PMIC Power Off Sequence Config 0 ^[3] 0 = Do Not Execute Config 0 1 = Execute Config 0 |
| 6 | RWPE | 0 | R58 [6]: POWER_OFF_SEQUENCE_CONFIG0_SWA_DISABLE Disable SWA Output Regulator. 0 = No Action 1 = Disable SWA Output Regulator |
| 5 | RWPE | 0 | R58 [5]: POWER_OFF_SEQUENCE_CONFIG0_SWB_DISABLE Disable Switch Node B Output Regulator. ^[4] 0 = No Action 1 = Disable SWB Output Regulator |
| 4 | RWPE | 0 | R58 [4]: POWER_OFF_SEQUENCE_CONFIG0_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = No Action 1 = Disable SWC Output Regulator |
| 3 | RWPE | 0 | R58 [3]: POWER_OFF_SEQUENCE_CONFIG0_SWD_DISABLE Disable SWD Output Regulator. 0 = No Action 1 = Disable SWD Output Regulator |
| 2:0 | RWPE | 0 | R58 [2:0]: POWER_OFF_SEQUENCE_CONFIG0_IDLE Idle time after Power Off Sequence Config 0 ^[5] 000 = 0 ms 001 = 1 ms 010 = 2 ms 011 = 3 ms 100 = 4 ms 101 = 5 ms 110 = 6 ms 111 = 7 ms |

NOTE 1 The PMIC always starts with power off sequence configuration 0 register and executes remaining power off sequence configuration registers (1 to 5) in sequential order.

NOTE 2 Power off sequence configuration 0 is total of 10 bit register. 8 bits as shown in [Table 256, Register 0x58 \[7:0\]](#) plus 2 bits in [Table 269, Register 0x65 \[7:6\]](#).

NOTE 3 If bit [7] = '0', bits [6:0] and [Table 269, Register 0x65 \[7:6\]](#) are ignored and PMIC moves to next power off sequence configuration register. If bit [7] = '1', PMIC executes bits [6:0] and [Table 269, Register 0x65 \[7:6\]](#) as configured; if no new rail is turned off, the PMIC simply waits the idle time as configured and then moves to next power off sequence configuration register.

NOTE 4 This register is only applicable if [Table 247, Register 0x4F \[5,0\]](#) = '00'. For any other setting in [Table 247, Register 0x4F \[5,0\]](#), this register does not apply and it is a don't care.

NOTE 5 Idle time is the additional time after soft-stop time expires. The PMIC waits sum of soft stop time and idle time before it executes the next power off sequence configuration register. If more than one regulators are disabled, the PMIC uses the largest value of the soft stop time among the regulators that are disabled in this configuration register.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 257 — Register 0x59

| R59 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7 | RWPE | 0 | R59 [7]: POWER_OFF_SEQUENCE_CONFIG1 PMIC Power Off Sequence Config1 ^[3] 0 = Do Not Execute Config 1 1 = Execute Config 1 |
| 6 | RWPE | 0 | R59 [6]: POWER_OFF_SEQUENCE_CONFIG1_SWA_DISABLE Disable SWA Output Regulator. 0 = No Action 1 = Disable SWA Output Regulator |
| 5 | RWPE | 0 | R59 [5]: POWER_OFF_SEQUENCE_CONFIG1_SWB_DISABLE Disable Switch Node B Output Regulator. ^[4] 0 = No Action 1 = Disable SWB Output Regulator |
| 4 | RWPE | 0 | R59 [4]: POWER_OFF_SEQUENCE_CONFIG1_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = No Action 1 = Disable SWC Output Regulator |
| 3 | RWPE | 0 | R59 [3]: POWER_OFF_SEQUENCE_CONFIG1_SWD_DISABLE Disable Switch Node D Output Regulator. 0 = No Action 1 = Disable SWD Output Regulator |
| 2:0 | RWPE | 0 | R59 [2:0]: POWER_OFF_SEQUENCE_CONFIG1_IDLE Idle time after Power Off Sequence Config 1 ^[5] 000 = 0 ms 001 = 1 ms 010 = 2 ms 011 = 3 ms 100 = 4 ms 101 = 5 ms 110 = 6 ms 111 = 7 ms |

NOTE 1 The PMIC always starts with power off sequence configuration 0 register and executes remaining power off sequence configuration registers (1 to 5) in sequential order.

NOTE 2 Power off sequence configuration 1 is total of 10 bit register. 8 bits as shown in [Table 257, Register 0x59](#) [7:0] plus 2 bits in [Table 269, Register 0x65](#) [5:4].

NOTE 3 If bit [7] = '0', bits [6:0] and [Table 269, Register 0x65](#) [5:4] are ignored and PMIC moves to next power off sequence configuration register. If bit [7] = '1', PMIC executes bits [6:0] and [Table 269, Register 0x65](#) [5:4] as configured; if no new rail is turned off, the PMIC simply waits the idle time as configured and then moves to next power off sequence configuration register.

NOTE 4 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 5 Idle time is the additional time after soft-stop time expires. The PMIC waits sum of soft stop time and idle time before it executes the next power off sequence configuration register. If more than one regulators are disabled, the PMIC uses the largest value of the soft stop time among the regulators that are disabled in this configuration register.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 258 — Register 0x5A

| R5A | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7 | RWPE | 0 | R5A [7]: POWER_OFF_SEQUENCE_CONFIG2 PMIC Power Off Sequence Config 2 ^[3] 0 = Do Not Execute Config 2 1 = Execute Config 2 |
| 6 | RWPE | 0 | R5A [6]: POWER_OFF_SEQUENCE_CONFIG2_SWA_DISABLE Disable SWA Output Regulator. 0 = No Action 1 = Disable SWA Output Regulator |
| 5 | RWPE | 0 | R5A [5]: POWER_OFF_SEQUENCE_CONFIG2_SWB_DISABLE Disable Switch Node B Output Regulator. ^[4] 0 = No Action 1 = Disable SWB Output Regulator |
| 4 | RWPE | 0 | R5A [4]: POWER_OFF_SEQUENCE_CONFIG2_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = No Action 1 = Disable SWC Output Regulator |
| 3 | RWPE | 0 | R5A [3]: POWER_OFF_SEQUENCE_CONFIG2_SWD_DISABLE Disable Switch Node D Output Regulator. 0 = No Action 1 = Disable SWD Output Regulator |
| 2:0 | RWPE | 0 | R5A [2:0]: POWER_OFF_SEQUENCE_CONFIG2_IDLE Idle time after Power Off Sequence Config 2 ^[5] 000 = 0 ms 001 = 1 ms 010 = 2 ms 011 = 3 ms 100 = 4 ms 101 = 5 ms 110 = 6 ms 111 = 7 ms |

NOTE 1 The PMIC always starts with power off sequence configuration 0 register and executes remaining power off sequence configuration registers (1 to 5) in sequential order.

NOTE 2 Power off sequence configuration 2 is total of 10 bit register. 8 bits as shown in [Table 258, Register 0x5A](#) [7:0] plus 2 bits in [Table 269, Register 0x65](#) [3:2].

NOTE 3 If bit [7] = '0', bits [6:0] and [Table 269, Register 0x65](#) [3:2] are ignored and PMIC moves to next power off sequence configuration register. If bit [7] = '1', PMIC executes bits [6:0] and [Table 269, Register 0x65](#) [3:2] as configured; if no new rail is turned off, the PMIC simply waits the idle time as configured and then moves to next power off sequence configuration register.

NOTE 4 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 5 Idle time is the additional time after soft-stop time expires. The PMIC waits sum of soft stop time and idle time before it executes the next power off sequence configuration register. If more than one regulators are disabled, the PMIC uses the largest value of the soft stop time among the regulators that are disabled in this configuration register.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 259 — Register 0x5B

| R5B | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7 | RWPE | 0 | R5B [7]: POWER_OFF_SEQUENCE_CONFIG3 PMIC Power Off Sequence Config 3 ^[3] 0 = Do Not Execute Config 3 1 = Execute Config 3 |
| 6 | RWPE | 0 | R5B [6]: POWER_OFF_SEQUENCE_CONFIG3_SWA_DISABLE Disable SWA Output Regulator. 0 = No Action 1 = Disable SWA Output Regulator |
| 5 | RWPE | 0 | R5B [5]: POWER_OFF_SEQUENCE_CONFIG3_SWB_DISABLE Disable SWB Output Regulator. ^[4] 0 = No Action 1 = Disable SWB Output Regulator |
| 4 | RWPE | 0 | R5B [4]: POWER_OFF_SEQUENCE_CONFIG3_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = No Action 1 = Disable SWC Output Regulator |
| 3 | RWPE | 0 | R5B [3]: POWER_OFF_SEQUENCE_CONFIG3_SWD_DISABLE Disable Switch Node D Output Regulator. 0 = No Action 1 = Disable SWD Output Regulator |
| 2:0 | RWPE | 0 | R5B [2:0]: POWER_OFF_SEQUENCE_CONFIG3_IDLE Idle time after Power Off Sequence Config 3 ^[5] 000 = 0 ms 001 = 1 ms 010 = 2 ms 011 = 3 ms 100 = 4 ms 101 = 5 ms 110 = 6 ms 111 = 7 ms |

NOTE 1 The PMIC always starts with power off sequence configuration 0 register and executes remaining power off sequence configuration registers (1 to 5) in sequential order.

NOTE 2 Power off sequence configuration 3 is total of 10 bit register. 8 bits as shown in [Table 259, Register 0x5B \[7:0\]](#) plus 2 bits in [Table 269, Register 0x65 \[1:0\]](#).

NOTE 3 If bit [7] = '0', bits [6:0] and [Table 269, Register 0x65 \[1:0\]](#) are ignored and PMIC moves to next power off sequence configuration register. If bit [7] = '1', PMIC executes bits [6:0] and [Table 269, Register 0x65 \[1:0\]](#) as configured; if no new rail is turned off, the PMIC simply waits the idle time as configured and then moves to next power off sequence configuration register.

NOTE 4 This register is only applicable if [Table 247, Register 0x4F \[5,0\]](#) = '00'. For any other setting in [Table 247, Register 0x4F \[5,0\]](#), this register does not apply and it is a don't care.

NOTE 5 Idle time is the additional time after soft-stop time expires. The PMIC waits sum of soft stop time and idle time before it executes the next power off sequence configuration register. If more than one regulators are disabled, the PMIC uses the largest value of the soft stop time among the regulators that are disabled in this configuration register.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 260 — Register 0x5C

| R5C | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7 | RWPE | 0 | R5C [7]: POWER_OFF_SEQUENCE_CONFIG4 PMIC Power Off Sequence Config 4 ^[3] 0 = Do Not Execute Config 4 1 = Execute Config 4 |
| 6 | RWPE | 0 | R5C [6]: POWER_OFF_SEQUENCE_CONFIG4_SWA_DISABLE Disable SWA Output Regulator. 0 = No Action 1 = Disable SWA Output Regulator |
| 5 | RWPE | 0 | R5C [5]: POWER_OFF_SEQUENCE_CONFIG4_SWB_DISABLE Disable SWB Output Regulator. ^[4] 0 = No Action 1 = Disable SWB Output Regulator |
| 4 | RWPE | 0 | R5C [4]: POWER_OFF_SEQUENCE_CONFIG4_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = No Action 1 = Disable SWC Output Regulator |
| 3 | RWPE | 0 | R5C [3]: POWER_OFF_SEQUENCE_CONFIG4_SWD_DISABLE Disable Switch Node D Output Regulator. 0 = No Action 1 = Disable SWD Output Regulator |
| 2:0 | RWPE | 0 | R5C [2:0]: POWER_OFF_SEQUENCE_CONFIG4_IDLE Idle time after Power Off Sequence Config 4 ^[5] 000 = 0 ms 001 = 1 ms 010 = 2 ms 011 = 3 ms 100 = 4 ms 101 = 5 ms 110 = 6 ms 111 = 7 ms |

NOTE 1 The PMIC always starts with power off sequence configuration 0 register and executes remaining power off sequence configuration registers (1 to 5) in sequential order.

NOTE 2 Power off sequence configuration 4 is total of 10 bit register. 8 bits as shown in [Table 260, Register 0x5C](#) [7:0] plus 2 bits in [Table 270, Register 0x66](#) [7:6].

NOTE 3 If bit [7] = '0', bits [6:0] and [Table 270, Register 0x66](#) [7:6] are ignored and PMIC moves to next power off sequence configuration register. If bit [7] = '1', PMIC executes bits [6:0] and [Table 270, Register 0x66](#) [7:6] as configured; if no new rail is turned off, the PMIC simply waits the idle time as configured and then moves to next power off sequence configuration register.

NOTE 4 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 5 Idle time is the additional time after soft-stop time expires. The PMIC waits sum of soft stop time and idle time before it executes the next power off sequence configuration register. If more than one regulators are disabled, the PMIC uses the largest value of the soft stop time among the regulators that are disabled in this configuration register.

11.6 DIMM Vendor Region Register Definition (cont'd)**Table 261 — Register 0x5D**

| R5D | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description |
| 7:5 | RWPE | 001 | R5D [7:5]: SWA_OUTPUT_SOFT_START_TIME SWA Output Regulator Soft Start Time After VR Enable ^[1] 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms ... 111 = 14 ms |
| 4 | RV | 0 | R5D [4]: Reserved |
| 3:1 | RWPE | 001 | R5D [3:1]: SWB_OUTPUT_SOFT_START_TIME SWB Output Regulator Soft Start Time After VR Enable ^{[1],[2]} 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms ... 111 = 14 ms |
| 0 | RV | 0 | R5D [0]: Reserved |

NOTE 1 This is the time it takes for buck regulator to go from 0 V to steady state voltage (the actual voltage varies based on pre-programmed voltage).

NOTE 2 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 262 — Register 0x5E

| R5E | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description |
| 7:5 | RWPE | 001 | R5E [7:5]: SWC_OUTPUT_SOFT_START_TIME SWC Output Regulator Soft Start Time After VR Enable ^[1] 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms ... 111 = 14 ms |
| 4 | RV | 0 | R5E [4]: Reserved |
| 3:1 | RWPE | 001 | R5E [3:1]: SWD_OUTPUT_SOFT_START_TIME SWD Output Regulator Soft Start Time After VR Enable ^[1] 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms ... 111 = 14 ms |
| 0 | RV | 0 | R5E [0]: Reserved |

NOTE 1 This is the time it takes for buck regulator to go from 0 V to steady state voltage (the actual voltage varies based on pre-programmed voltage)

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 263 — Register 0x5F

| R5F | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description |
| 7 | RWPE | 0 | R5F [7]: R2F_2_CONTROL Host Region R2F[2] Register Setting at First Power On 0 = R2F[2] = '0' 1 = R2F[2] = '1' |
| 6 | RWPE | 0 | R5F [6]: PMIC_AUTO_POWER_EN PMIC Auto Power On Control ^{[1],[2]} 0 = PMIC requires VR Enable command to turn on output rails 1 = PMIC automatically powers on output rails as soon as it detects valid VIN_Bulk and VIN_Mgmt input supplies ^[3] |
| 5 | RWPE | 0 | R5F [5]: VR_OE_ENABLE VR Output Enable 0 = VR OE pin function is disabled ^{[4],[5]} 1 = VR OE pin function is enabled. PMIC turns on SWx when VR_OE pin is asserted High and turns off the SWx when VR_OE pin is de-asserted ^[6] |
| 4 | RWPE | 0 | R5F [4]: R32_4_CONTROL Host Region R32[4] Register Setting at First Power On 0 = R32[4] = '0' 1 = R32[4] = '1' |
| 3:0 | RV | 0 | R5F [3:0]: Reserved |

NOTE 1 The PMIC considers the setting of bits [6:5] = '11' as illegal.

NOTE 2 When this feature is enabled, it takes in effect at next power cycle.

NOTE 3 Once the PMIC output rails are powered up, if there is a subsequent VR Disable command or a fault event, the PMIC output regulators remains off until subsequent VR Enable command.

NOTE 4 When this feature is enabled, the VR_OE input pin must be held low. The enable function takes in effect at next power cycle.

NOTE 5 PMIC does not turn on the rail when VR_OE pin is high however the PMIC does turn off the regulator when VR_OE pin is low. The PMIC is prevented from turning on the regulators as long as VR_OE pin is low.

NOTE 6 At initial power on, the VR_OE pin must be held low while VIN_Bulk and VIN_Mgmt input supplies are ramping up.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 264 — Register 0x60

| R60 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description |
| 7:5 | RWPE | 001 | R60 [7:5]: SWE_OUTPUT_SOFT_START_TIME SWE Output Regulator Soft Start Time After VR Enable ^{[1],[2]} 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms ... 111 = 14 ms |
| 4 | RV | 0 | R60 [4]: Reserved |
| 3:1 | RWPE | 001 | R60 [3:1]: SWF_OUTPUT_SOFT_START_TIME SWF Output Regulator Soft Start Time After VR Enable ^{[1],[3]} 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms ... 111 = 14 ms |
| 0 | RV | 0 | R60 [0]: Reserved |

NOTE 1 This is the time it takes for buck regulator to go from 0 V to steady state voltage (the actual voltage varies based on pre-programmed voltage).

NOTE 2 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00' or '01'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 3 This register is only applicable if [Table 247, Register 0x4F](#) [6] = '0'. For any other setting in [Table 247, Register 0x4F](#) [6], this register does not apply and it is a don't care.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 265 — Register 0x61

| R61 | | | |
|------|-----------|---------|---|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7 | RWPE | 0 | R61 [7]: POWER_ON_SEQUENCE_CONFIG5 PMIC Power On Sequence Config 5 0 = Do Not Execute Config 5 ^[3] 1 = Execute Config 5 |
| 6 | RWPE | 0 | R61 [6]: POWER_ON_SEQUENCE_CONFIG5_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = No Action 1 = Enable Switch Node A Output Regulator |
| 5 | RWPE | 0 | R61 [5]: POWER_ON_SEQUENCE_CONFIG5_SWB_ENABLE Enable Switch Node B Output Regulator. ^[4] 0 = No Action 1 = Enable Switch Node B Output Regulator |
| 4 | RWPE | 0 | R61 [4]: POWER_ON_SEQUENCE_CONFIG5_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = No Action 1 = Enable Switch Node C Output Regulator |
| 3 | RWPE | 0 | R61 [3]: POWER_ON_SEQUENCE_CONFIG5_SWD_ENABLE Enable Switch Node D Output Regulator. 0 = No Action 1 = Enable Switch Node D Output Regulator |
| 2:0 | RWPE | 001 | R61 [2:0]: POWER_ON_SEQUENCE_CONFIG5_IDLE Idle time after Power On Sequence Config 5 ^[5] 000 = 0 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms 100 = 8 ms 101 = 10 ms 110 = 12 ms 111 = 24 ms |

NOTE 1 The PMIC always starts with power on sequence configuration 0 register and executes remaining power on sequence configuration registers (1 to 5) in sequential order.

NOTE 2 Power on sequence configuration 5 is total of 10 bit register. 8 bits as shown in [Table 265, Register 0x61](#) [7:0] plus 2 bits in [Table 268, Register 0x64](#) [5:4].

NOTE 3 If bit [7] = '0', bits [6:0] [Table 268, Register 0x64](#) [5:4] are ignored and PMIC moves to next power on sequence configuration register. If bit [7] = '1', PMIC executes bits [6:0] [Table 268, Register 0x64](#) [5:4] as configured; if no new rail is turned on, the PMIC simply waits the idle time as configured and then moves to next power sequence configuration register.

NOTE 4 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 5 Idle time is the additional time after soft-start time expires. The PMIC waits sum of Soft Start time and Idle time before it executes the next event. If more than one regulators are enabled, the PMIC uses the largest value of the soft start time among the regulators that are enabled in this configuration register.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 266 — Register 0x62

| R62 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^{[1],[2]} |
| 7 | RWPE | 0 | R62 [7]: POWER_OFF_SEQUENCE_CONFIG5 PMIC Power Off Sequence Config 5 ^[3] 0 = Do Not Execute Config 5 1 = Execute Config 5 |
| 6 | RWPE | 0 | R62 [6]: POWER_OFF_SEQUENCE_CONFIG5_SWA_DISABLE Disable SWA Output Regulator. 0 = No Action 1 = Disable SWA Output Regulator |
| 5 | RWPE | 0 | R62 [5]: POWER_OFF_SEQUENCE_CONFIG5_SWB_DISABLE Disable SWB Output Regulator. ^[4] 0 = No Action 1 = Disable SWB Output Regulator |
| 4 | RWPE | 0 | R62 [4]: POWER_OFF_SEQUENCE_CONFIG5_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = No Action 1 = Disable SWC Output Regulator |
| 3 | RWPE | 0 | R62 [3]: POWER_OFF_SEQUENCE_CONFIG5_SWD_DISABLE Disable Switch Node D Output Regulator. 0 = No Action 1 = Disable SWD Output Regulator |
| 2:0 | RWPE | 0 | R62 [2:0]: POWER_OFF_SEQUENCE_CONFIG5_IDLE Idle time after Power Off Sequence Config 5 ^[5] 000 = 0 ms 001 = 1 ms 010 = 2 ms 011 = 3 ms 100 = 4 ms 101 = 5 ms 110 = 6 ms 111 = 7 ms |

NOTE 1 The PMIC always starts with power off sequence configuration 0 register and executes remaining power off sequence configuration registers (1 to 5) in sequential order.

NOTE 2 Power off sequence configuration 5 is total of 10 bit register. 8 bits as shown in [Table 266, Register 0x62](#) [7:0] plus 2 bits in [Table 270, Register 0x66](#) [5:4].

NOTE 3 If bit [7] = '0', bits [6:0] and [Table 270, Register 0x66](#) [5:4] are ignored and PMIC moves to next power off sequence configuration register. If bit [7] = '1', PMIC executes bits [6:0] and [Table 270, Register 0x66](#) [5:4] as configured; if no new rail is turned off, the PMIC simply waits the idle time as configured and then moves to next power off sequence configuration register.

NOTE 4 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 5 Idle time is the additional time after soft-stop time expires. The PMIC waits sum of soft stop time and idle time before it executes the next power off sequence configuration register. If more than one regulators are disabled, the PMIC uses the largest value of the soft stop time among the regulators that are disabled in this configuration register.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 267 — Register 0x63

| R63 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^[1] |
| 7 | RWPE | 0 | R63 [7]: POWER_ON_SEQUENCE_CONFIG0_EXT_SWE_ENABLE PMIC Power On Sequence Config0 Extension ^[2] 0 = No Action 1 = Enable SWE Output Regulator |
| 6 | RWPE | 0 | R63 [6]: POWER_ON_SEQUENCE_CONFIG0_EXT_SWF_ENABLE PMIC Power On Sequence Config0 Extension ^[3] 0 = No Action 1 = Enable SWF Output Regulator |
| 5 | RWPE | 0 | R63 [5]: POWER_ON_SEQUENCE_CONFIG1_EXT_SWE_ENABLE PMIC Power On Sequence Config1 Extension ^[2] 0 = No Action 1 = Enable SWE Output Regulator |
| 4 | RWPE | 0 | R63 [4]: POWER_ON_SEQUENCE_CONFIG1_EXT_SWF_ENABLE PMIC Power On Sequence Config1 Extension ^[3] 0 = No Action 1 = Enable SWF Output Regulator |
| 3 | RWPE | 0 | R63 [3]: POWER_ON_SEQUENCE_CONFIG2_EXT_SWE_ENABLE PMIC Power On Sequence Config2 Extension ^[2] 0 = No Action 1 = Enable SWE Output Regulator |
| 2 | RWPE | 0 | R63 [2]: POWER_ON_SEQUENCE_CONFIG2_EXT_SWF_ENABLE PMIC Power On Sequence Config2 Extension ^[3] 0 = No Action 1 = Enable SWF Output Regulator |
| 1 | RWPE | 0 | R63 [1]: POWER_ON_SEQUENCE_CONFIG3_EXT_SWE_ENABLE PMIC Power On Sequence Config3 Extension ^[2] 0 = No Action 1 = Enable SWE Output Regulator |
| 0 | RWPE | 0 | R63 [0]: POWER_ON_SEQUENCE_CONFIG3_EXT_SWF_ENABLE PMIC Power On Sequence Config3 Extension ^[3] 0 = No Action 1 = Enable SWF Output Regulator |

NOTE 1 Power on sequence configuration 0 to 3 registers are total of 10 bit register. 8 bits as shown in [Table 232, Register 0x40](#) to [Table 235, Register 0x43](#) plus 2 bits as shown in this register.

NOTE 2 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00' or '01'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 3 This register is only applicable if [Table 247, Register 0x4F](#) [6] = '0'. For any other setting in [Table 247, Register 0x4F](#) [6], this register does not apply and it is a don't care.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 268 — Register 0x64

| R64 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^[1] |
| 7 | RWPE | 0 | R64 [7]: POWER_ON_SEQUENCE_CONFIG4_EXT_SWE_ENABLE PMIC Power On Sequence Config4 Extension ^[2] 0 = No Action 1 = Enable SWE Output Regulator |
| 6 | RWPE | 0 | R64 [6]: POWER_ON_SEQUENCE_CONFIG4_EXT_SWF_ENABLE PMIC Power On Sequence Config4 Extension ^[3] 0 = No Action 1 = Enable SWF Output Regulator |
| 5 | RWPE | 0 | R64 [5]: POWER_ON_SEQUENCE_CONFIG5_EXT_SWE_ENABLE PMIC Power On Sequence Config5 Extension ^[2] 0 = No Action 1 = Enable SWE Output Regulator |
| 4 | RWPE | 0 | R64 [4]: POWER_ON_SEQUENCE_CONFIG5_EXT_SWF_ENABLE PMIC Power On Sequence Config5 Extension ^[3] 0 = No Action 1 = Enable SWF Output Regulator |
| 3:0 | RV | 0 | R64 [3:0]: Reserved |

NOTE 1 Power on sequence configuration 4 to 5 registers are total of 10 bit register. 8 bits as shown in [Table 236, Register 0x44](#), [Table 265, Register 0x61](#) plus 2 bits as shown in this register.

NOTE 2 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00' or '01'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 3 This register is only applicable if [Table 247, Register 0x4F](#) [6] = '0'. For any other setting in [Table 247, Register 0x4F](#) [6], this register does not apply and it is a don't care.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 269 — Register 0x65

| R65 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^[1] |
| 7 | RWPE | 0 | R65 [7]: POWER_OFF_SEQUENCE_CONFIG0_EXT_SWE_DISABLE PMIC Power Off Sequence Config0 Extension ^[2] 0 = No Action 1 = Disable SWE Output Regulator |
| 6 | RWPE | 0 | R65 [6]: POWER_OFF_SEQUENCE_CONFIG0_EXT_SWF_DISABLE PMIC Power Off Sequence Config0 Extension ^[3] 0 = No Action 1 = Disable SWF Output Regulator |
| 5 | RWPE | 0 | R65 [5]: POWER_OFF_SEQUENCE_CONFIG1_EXT_SWE_DISABLE PMIC Power Off Sequence Config1 Extension ^[2] 0 = No Action 1 = Disable SWE Output Regulator |
| 4 | RWPE | 0 | R65 [4]: POWER_OFF_SEQUENCE_CONFIG1_EXT_SWF_DISABLE PMIC Power Off Sequence Config1 Extension ^[3] 0 = No Action 1 = Disable SWF Output Regulator |
| 3 | RWPE | 0 | R65 [3]: POWER_OFF_SEQUENCE_CONFIG2_EXT_SWE_DISABLE PMIC Power Off Sequence Config2 Extension ^[2] 0 = No Action 1 = Disable SWE Output Regulator |
| 2 | RWPE | 0 | R65 [2]: POWER_OFF_SEQUENCE_CONFIG2_EXT_SWF_DISABLE PMIC Power Off Sequence Config2 Extension ^[3] 0 = No Action 1 = Disable SWF Output Regulator |
| 1 | RWPE | 0 | R65 [1]: POWER_OFF_SEQUENCE_CONFIG3_EXT_SWE_DISABLE PMIC Power Off Sequence Config3 Extension ^[2] 0 = No Action 1 = Disable SWE Output Regulator |
| 0 | RWPE | 0 | R65 [0]: POWER_OFF_SEQUENCE_CONFIG3_EXT_SWF_DISABLE PMIC Power Off Sequence Config3 Extension ^[3] 0 = No Action 1 = Disable SWF Output Regulator |

NOTE 1 Power off sequence configuration 0 to 3 registers are total of 10 bit register. 8 bits as shown in [Table 256, Register 0x58](#) to [Table 259, Register 0x5B](#) plus 2 bits as shown in this register.

NOTE 2 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00' or '01'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 3 This register is only applicable if [Table 247, Register 0x4F](#) [6] = '0'. For any other setting in [Table 247, Register 0x4F](#) [6], this register does not apply and it is a don't care.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 270 — Register 0x66

| R66 | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description ^[1] |
| 7 | RWPE | 0 | R66 [7]: POWER_OFF_SEQUENCE_CONFIG4_EXT_SWE_DISABLE PMIC Power Off Sequence Config4 Extension ^[2] 0 = No Action 1 = Disable SWE Output Regulator |
| 6 | RWPE | 0 | R66 [6]: POWER_OFF_SEQUENCE_CONFIG4_EXT_SWF_DISABLE PMIC Power Off Sequence Config4 Extension ^[3] 0 = No Action 1 = Disable SWF Output Regulator |
| 5 | RWPE | 0 | R66 [5]: POWER_OFF_SEQUENCE_CONFIG5_EXT_SWE_DISABLE PMIC Power Off Sequence Config5 Extension ^[2] 0 = No Action 1 = Disable SWE Output Regulator |
| 4 | RWPE | 0 | R66 [4]: POWER_OFF_SEQUENCE_CONFIG5_EXT_SWF_DISABLE PMIC Power Off Sequence Config5 Extension ^[3] 0 = No Action 1 = Disable SWF Output Regulator |
| 3:0 | RV | 0 | R66 [3:0]: Reserved |

NOTE 1 Power off sequence configuration 4 to 5 registers are total of 10 bit register. 8 bits as shown in [Table 260, Register 0x5C](#), [Table 266, Register 0x62](#) plus 2 bits as shown in this register.

NOTE 2 This register is only applicable if [Table 247, Register 0x4F](#) [5,0] = '00' or '01'. For any other setting in [Table 247, Register 0x4F](#) [5,0], this register does not apply and it is a don't care.

NOTE 3 This register is only applicable if [Table 247, Register 0x4F](#) [6] = '0'. For any other setting in [Table 247, Register 0x4F](#) [6], this register does not apply and it is a don't care.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 271 — Register 0x67

| R67 | | | |
|------|-----------|--------------|---|
| Bits | Attribute | Default | Description |
| 7:0 | RWPE | 0011 1100 | <p>R67 [7:0]: SWA_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD SWA Output High Current Consumption Warning Threshold^[1]</p> <p>If Table 155, Register 0x32[1:0] = '00': 0000 0000 = Undefined 0000 0001 \geq 125 mA 0000 0010 \geq 250 mA ... 1111 1111 \geq 31.875 A</p> <p>If Table 155, Register 0x32[1:0] = '01': 0000 0000 = Undefined 0000 0001 \geq 31.25 mA 0000 0010 \geq 62.5 mA ... 1111 1111 \geq 7.968 A</p> |

NOTE 1 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [5,0]. For dual phase operation, registers [Table 271, Register 0x67](#) [7:0] and [Table 272, Register 0x68](#) [7:0] must be configured identical. For three phase operation, registers [Table 271, Register 0x67](#) [7:0], [Table 272, Register 0x68](#) [7:0], and [Table 275, Register 0x6B](#) [7:0] must be configured identical.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 272 — Register 0x68

| R68 | | | |
|------|-----------|--------------|--|
| Bits | Attribute | Default | Description |
| 7:0 | RWPE | 0011 1100 | <p>R68 [7:0]: SWB_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD SWB Output High Current Consumption Warning Threshold^[1]</p> <p>If Table 155, Register 0x32[1:0] = '00': 0000 0000 = Undefined 0000 0001 \geq 125 mA 0000 0010 \geq 250 mA ... 1111 1111 = > 31.875 A</p> <p>If Table 155, Register 0x32[1:0] = '01': 0000 0000 = Undefined 0000 0001 \geq 31.25 mA 0000 0010 \geq 62.5 mA ... 1111 1111 \geq 7.968 A</p> |

NOTE 1 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [5,0]. For dual phase operation, registers [Table 271, Register 0x67](#) [7:0] and [Table 272, Register 0x68](#) [7:0] must be configured identical. For three phase operation, registers [Table 271, Register 0x67](#) [7:0], [Table 272, Register 0x68](#) [7:0], and [Table 275, Register 0x6B](#) [7:0] must be configured identical.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 273 — Register 0x69

| R69 | | | |
|------|-----------|--------------|---|
| Bits | Attribute | Default | Description |
| 7:0 | RWPE | 0011 1100 | <p>R69 [7:0]: SWC_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD SWC Output High Current Consumption Warning Threshold^[1]</p> <p>If Table 155, Register 0x32[1:0] = '00': 0000 0000 = Undefined 0000 0001 \geq 125 mA 0000 0010 \geq 250 mA ... 1111 1111 \geq 31.875 A</p> <p>If Table 155, Register 0x32[1:0] = '01': 0000 0000 = Undefined 0000 0001 \geq 31.25 mA 0000 0010 \geq 62.5 mA ... 1111 1111 \geq 7.968 A</p> |

NOTE 1 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [6]. For dual phase operation, registers [Table 273, Register 0x69](#) [7:0] and [Table 276, Register 0x6C](#) [7:0] must be configured identical.

Table 274 — Register 0x6A

| R6A | | | |
|------|-----------|--------------|---|
| Bits | Attribute | Default | Description |
| 7:0 | RWPE | 0010 1000 | <p>R6A [7:0]: SWD_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD SWD Output High Current Consumption Warning Threshold</p> <p>If Table 155, Register 0x32[1:0] = '00': 0000 0000 = Undefined 0000 0001 \geq 125 mA 0000 0010 \geq 250 mA ... 1111 1111 \geq 31.875 A</p> <p>If Table 155, Register 0x32[1:0] = '01': 0000 0000 = Undefined 0000 0001 \geq 31.25 mA 0000 0010 \geq 62.5 mA ... 1111 1111 \geq 7.968 A</p> |

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 275 — Register 0x6B

| R6B | | | |
|------|-----------|--------------|---|
| Bits | Attribute | Default | Description |
| 7:0 | RWPE | 0011 1100 | <p>R6B [7:0]: SWE_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD SWE Output High Current Consumption Warning Threshold^[1]</p> <p>If Table 155, Register 0x32[1:0] = '00': 0000 0000 = Undefined 0000 0001 \geq 125 mA 0000 0010 \geq 250 mA ... 1111 1111 \geq 31.875 A</p> <p>If Table 155, Register 0x32[1:0] = '01': 0000 0000 = Undefined 0000 0001 \geq 31.25 mA 0000 0010 \geq 62.5 mA ... 1111 1111 \geq 7.968 A</p> |

NOTE 1 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [5,0]. For three phase operation, registers [Table 271, Register 0x67](#) [7:0], [Table 272, Register 0x68](#) [7:0], and [Table 275, Register 0x6B](#) [7:0] must be configured identical.

Table 276 — Register 0x6C

| R6C | | | |
|------|-----------|--------------|---|
| Bits | Attribute | Default | Description |
| 7:0 | RWPE | 0011 1100 | <p>R6C [7:0]: SWF_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD SWF Output High Current Consumption Warning Threshold^[1]</p> <p>If Table 155, Register 0x32[1:0] = '00': 0000 0000 = Undefined 0000 0001 \geq 125 mA 0000 0010 \geq 250 mA ... 1111 1111 \geq 31.875 A</p> <p>If Table 155, Register 0x32[1:0] = '01': 0000 0000 = Undefined 0000 0001 \geq 31.25 mA 0000 0010 \geq 62.5 mA ... 1111 1111 \geq 7.968 A</p> |

NOTE 1 This register is applicable regardless of the setting in [Table 247, Register 0x4F](#) [6]. For dual phase operation, registers [Table 273, Register 0x69](#) [7:0] and [Table 276, Register 0x6C](#) [7:0] must be configured identical.

11.6 DIMM Vendor Region Register Definition (cont'd)

Table 277 — Register 0x6F

| R6F | | | |
|------|-----------|---------|--|
| Bits | Attribute | Default | Description |
| 7:0 | RWPE | - | R6F [7:0]: DIMM_VENDOR_REGION_CRC_CODE DIMM Vendor Region 8-bit CRC Code ^{[1],[2]} |

- NOTE 1 Programmed by DIMM vendor during DIMM assembly.
- NOTE 2 See Clause 6.30 for CRC code computation procedure.

12 Package Drawings

12.1 Mechanical Outline Drawing

Figure 36, Figure 37, and Figure 38 show the PMIC package mechanical outline drawing.

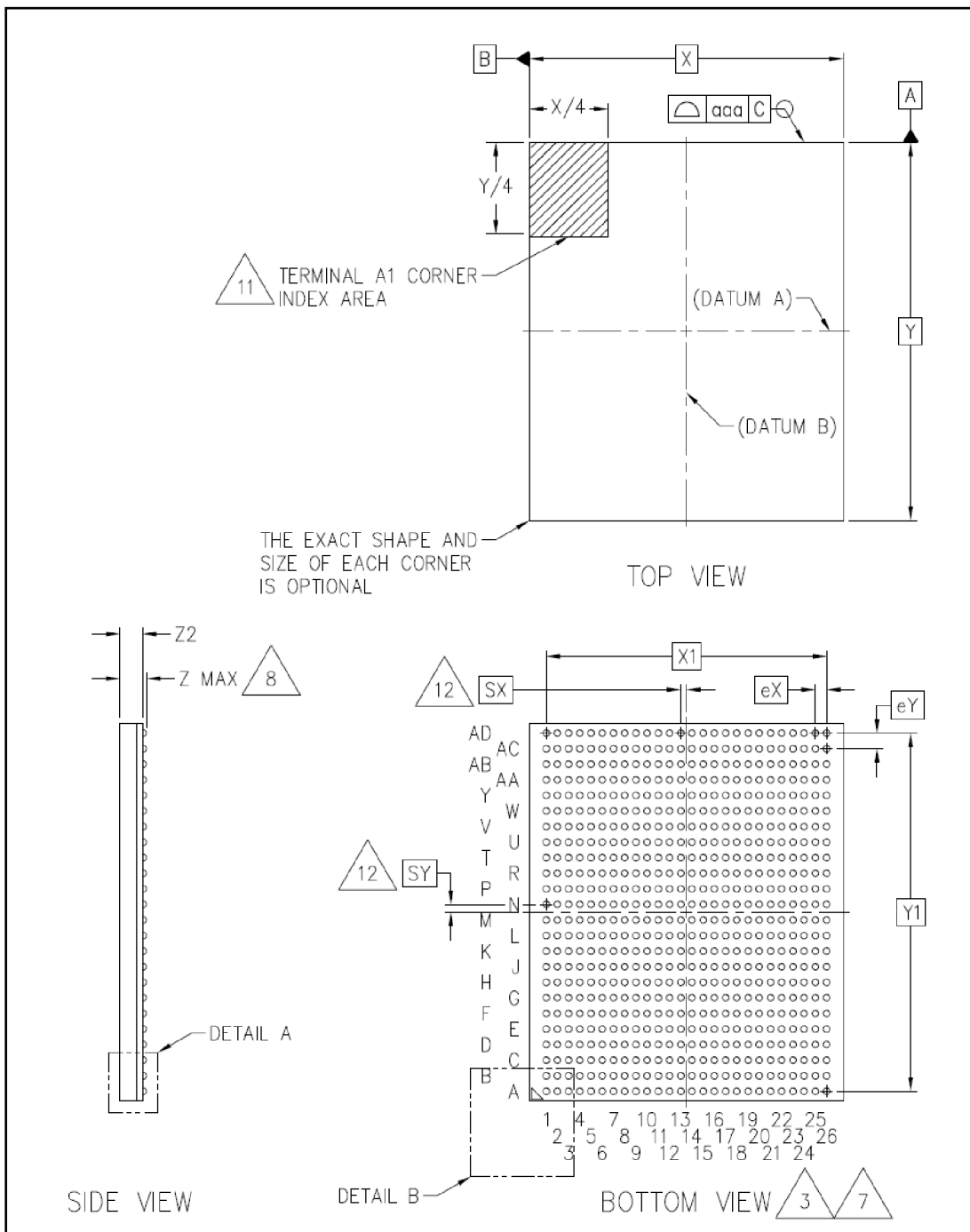


Figure 36 — Package Mechanical Outline

12.1 Mechanical Outline Drawing (cont'd)

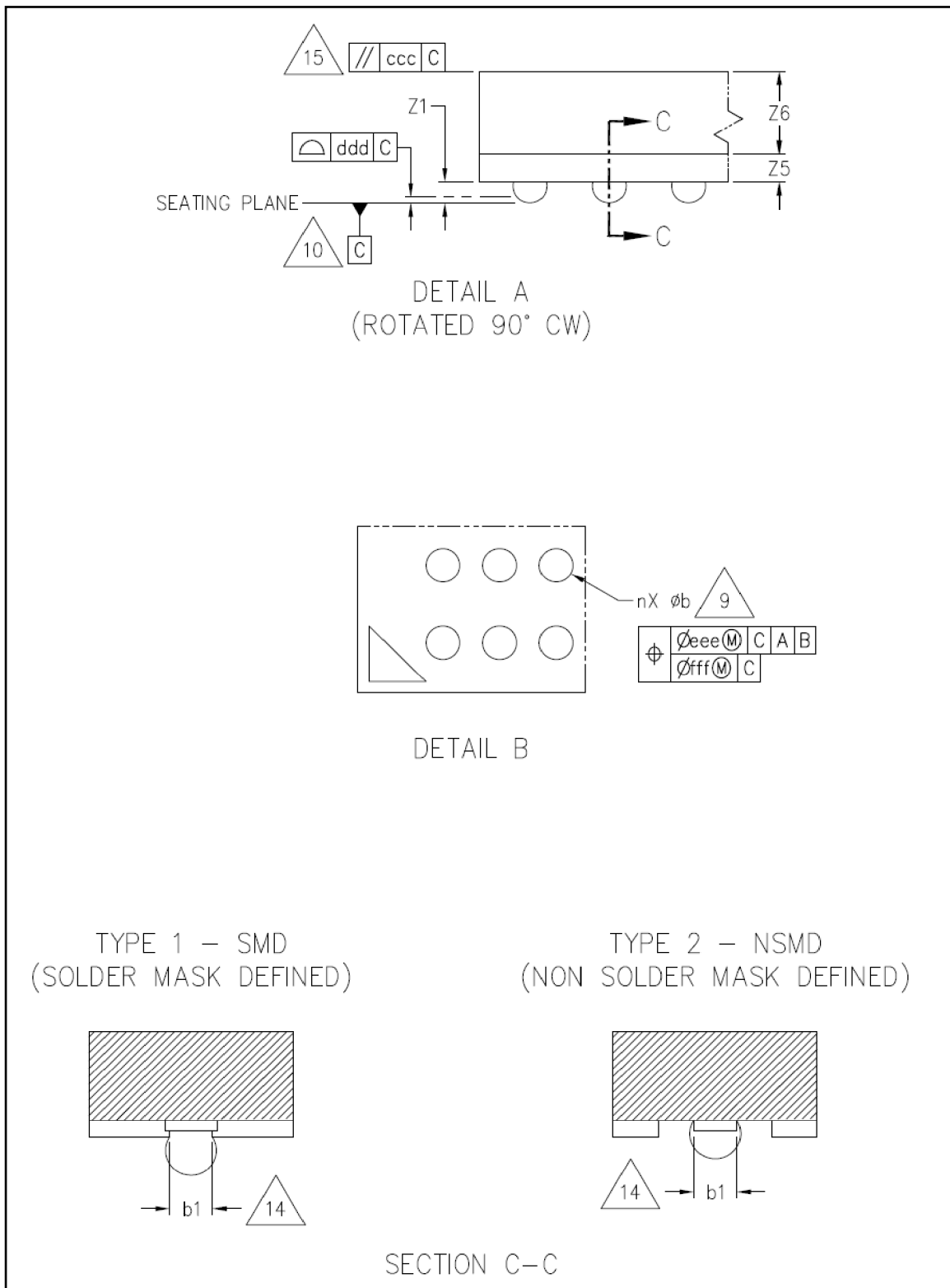


Figure 37 — Detail A, Detail B Drawings

12.1 Mechanical Outline Drawing (cont'd)

TABLE 1

| COMMON DIMENSIONS | | |
|-------------------|-------------------------|---------------------------------------|
| SYMBOL | | |
| Z | | PACKAGE SPECIFIC |
| Z2 | $b(\text{NOM}) = 0.300$ | $Z2(\text{MAX}) = Z(\text{MAX}) - Z1$ |
| Z5 | | OPTIONAL – PACKAGE SPECIFIC |
| Z6 | | OPTIONAL – PACKAGE SPECIFIC |
| eX | | 0.50 BASIC |
| eY | | 0.70 BASIC |
| NOTES | | 1, 2, 8 |
| REF | | 11–1048A |
| ISSUE | | A |

TABLE 2


| COMMON DIMENSIONS | | | |
|-------------------|----------------------|-------|-------|
| SYMBOL | SOLDER BALL DIAMETER | | |
| | MIN | NOM | MAX |
| Z1 | PACKAGE SPECIFIC | --- | --- |
| b | 0.225 | 0.300 | 0.375 |
| b1 | TYPE 1 | 0.20 | --- |
| | TYPE 2 | 0.20 | --- |
| NOTES | | | |
| 1, 2, 17 | | | |
| REF | | | |
| 11–1048A | | | |
| ISSUE | | | |
| A | | | |

TABLE 3

| TOLERANCE OF FORM AND POSITION | | |
|--------------------------------|--------------|------------------------------|
| SYMBOL | PACKAGE TYPE | VALUE |
| | | $\phi b \text{ NOM} = 0.300$ |
| aaa | --- | 0.10 |
| ccc | ENCAPSULATED | 0.20 |
| ddd | --- | 0.08 |
| eee | ENCAPSULATED | 0.15 |
| fff | --- | 0.05 |
| NOTES | | |
| 1, 2 | | |
| REF | | |
| 11–1048A | | |
| ISSUE | | |
| A | | |

Figure 38 — Common Dimension and Tolerances

12.1 Mechanical Outline Drawing (cont'd)

| TABLE 4 | | | | | | | | | | | | | | |
|--|---|------------|------------|-------------|-------------|----|----|-------------|-------------|-------|-----|---------------------|----------|-------|
| øb = 0.300 NOMINAL | | | | | | | | | | | | | | |
| VARIATION |  | X BASIC | Y BASIC | X1 BASIC | Y1 BASIC | MX | MY | SX BASIC | SY BASIC | n | N | TERMINAL PATTERN | REF | ISSUE |
| PBGA-B113[143]_J0p5-R5p55x9p0Z#-C0p3Z# | | 5.55 | 9.00 | 5.00 | 8.40 | 11 | 13 | 0.00 | 0.00 | 113 | 143 | A | 11-1048A | A |
| | | | | | | | | | | | | | | |
| | | 2 | 2 | 2 | 2 | 5 | 5 | 2, 12 | 2, 12 | 6, 13 | 6 | 13 | | |

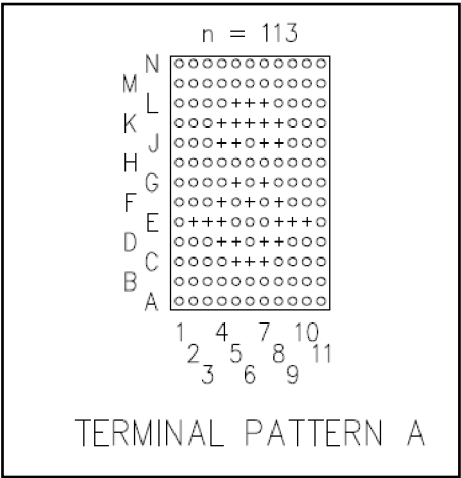


Figure 39 — Terminal Pattern



Standard Improvement Form**JEDEC Standard JESD301-5**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

| |
|--|
| |
| |
| |
| |

3. Other suggestions for document improvement:

| |
|--|
| |
| |
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Date: _____

